GaAs MQW Modulators Integrated with Silicon CMOS

K. W. Goossen, *Member, IEEE,* J. A. Walker, L. A. D'Asaro, *Life Senior Member, IEEE,* S. P. Hui, B. Tseng, R. Leibenguth, D. Kossives, D. D. Bacon, D. Dahringer, L. M. F. Chirovsky, A. L. Lentine, *Member, IEEE,* and D. A. B. Miller, *Fellow, IEEE*

***Abstract*—We demonstrate integration of GaAs–AlGaAs multiple quantum well modulators to silicon CMOS circuitry via flip-chip solder-bonding followed by substrate removal. We obtain 95% device yield for 32 × 32 arrays of devices with 15 micron solder pads. We show operation of a simple circuit composed of a modulator and a CMOS transistor.**

I. Introduction

FOR many years now a much desired goal of those working on optical interconnects and optical computing has been the integration of high density silicon electronics with high performance GaAs-based optoelectronics. In particular, the possibility of direct optical communication to logic chips has stimulated much work on photonic switching [1]. The most desirable product is one where the silicon circuitry is state-of-the-art, and unaffected by the integration with the optoelectronics. For this reason flip-chip solder bonding to finished silicon chips has been pursued [2]. Furthermore, modulators, which can be fabricated in densities of thousand per chip [3], are the preferred optoelectronic component in many *systems* such as in [1]. Finally, GaAs–AlGaAs multiple quantum well modulators operating at 850 nm offer the highest performance compared to longer wavelength modulators [4], [5].

In [6], we demonstrated that the GaAs substrate could be removed after flip-chip bonding, allowing operation at 850 nm. This procedure of bonding, followed by substrate removal, has been explored in detail by us, and here we present its application to silicon CMOS, thus fulfilling the above-stated goal. We demonstrate here a 99.9% bond yield with a steadily improving 95% device yield. Furthermore, all aspects of this procedure appear to fit within a manufacturable scheme, with no thin-film handling required as in epitaxial lift-off [7]. We have even demonstrated that completed chips can be sawed without damage, allowing batch fabrication of many chips at once. In [6], the devices operated at high optical intensity (80 kW/cm^2), a huge thermal flux and electrical current density, showing excellent heat-sinking and ohmic contact. The device was thermally cycled from 30 °C to 100 °C over a hundred times, and it showed no degradation, showing the practicality of the technique.

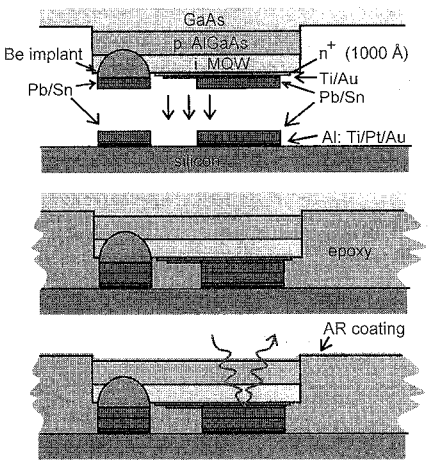

Fig. 1. Three-step hybridization process: 1) Fabrication, aligning, and bonding of modulator chip on silicon chip. 2) Flowing etch-protectant between chips, which is allowed to harden. 3) Removal of GaAs substrate using jet etcher, and deposition of AR coating. The epoxy can be removed after substrate removal, as desired.

The fabrication procedure is outlined in Fig. 1. Modulators are produced in the GaAs chip whose n and p contacts are coplanar. In [6] this was accomplished by depositing thick gold over the bottom contact. Here we employ implantation [8]. Lead-tin is deposited on these for a solder using photolithography. The silicon chips are obtained from the MOSIS foundry facility. The chip have 1.2 micron linerules. Mating aluminum pads from the modulators are designed on those chips, and a Ti–Pt–Au layer is deposited on them (in our lab) to provide a solder-wettable surface. A precision bonder made by Research Devices in Piscataway, NJ was employed to bond the chips together. Two-micron accuracy is routine.

A key feature of the technique for flip-chip bonding then substrate removal is the etching of outer mesas around the devices into the substrate. Then, when the substrate is removed by applying a chemical stream to it (that stops on the AlGaAs stop-etch layer), isolated devices will be left. This is desirable since, if the stop etch layer was left extending over the whole chip, slight warpages would cause it to break, possibly damaging the modulators. This procedure requires placing something between the mesas so that the substrate etchant does not attack the front faces of the chips. The substrate etchant, 100:1 H_2O_2:NH_4OH, does not attack Si or Al appreciably.

Manuscript received November 1, 1994; revised December 9, 1994.

K. W. Goossen, J. A. Walker, and D. A. B. Miller are with AT&T Bell Laboratories, Holmdel, NJ 07733 USA.

L. A. D'Asaro, S. P. Hui, B. Tseng, R. Leibenguth, D. Kossives, D. Dahringer, and L. M. F. Chirovsky are with AT&T Bell Laboratories, Murray Hill, NJ 07974 USA.

A. L. Lentine is with AT&T Bell Laboratories, Naperville, IL 60566 USA.

IEEE Log Number 9409250.

1041–1135/95$04.00 © 1995 IEEE

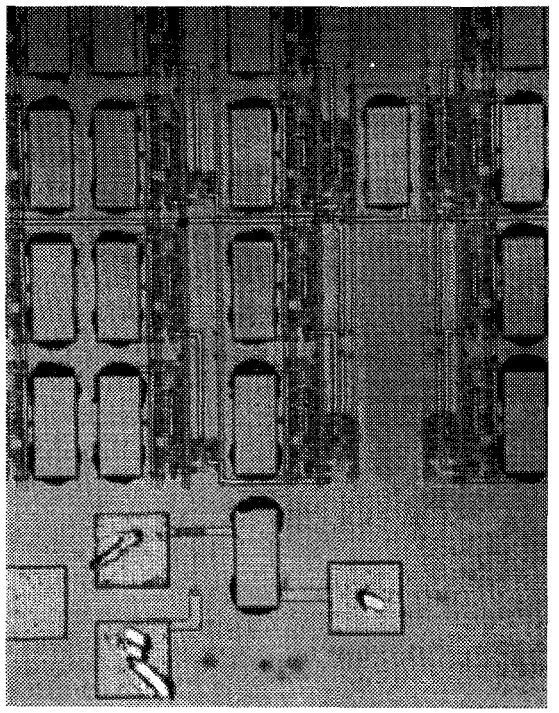

Fig. 2. Photo of integrated GaAs modulators on silicon CMOS. Results on the transistor modulator circuit (near bottom of photo) are presented here. Results on the complex circuits will be reported later.

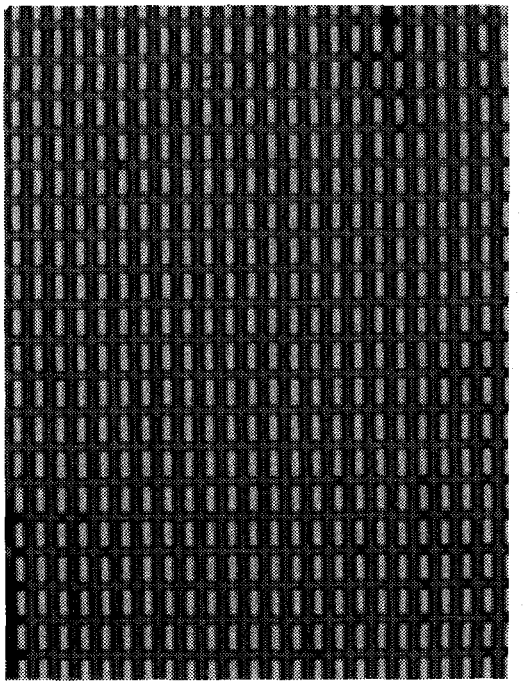

Fig. 3. GaAs modulator test array on silicon.

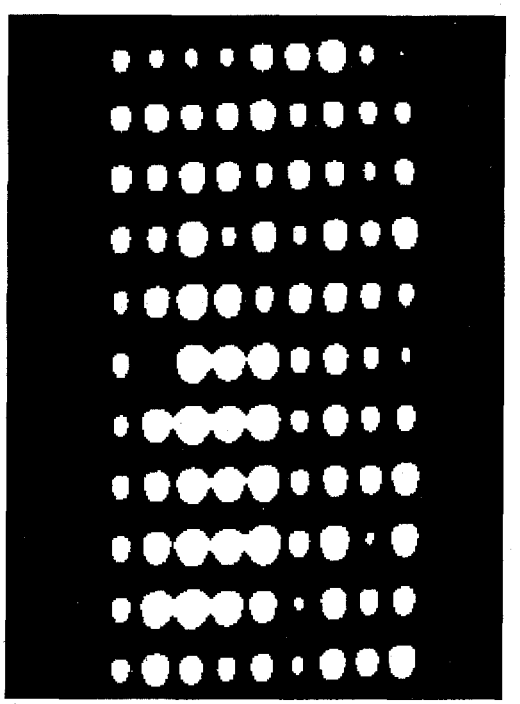

Fig. 4. Best section of LED (forward-biased modulator) array with 98/99 working devices.

However, it would attack the GaAs regions of the modulators. To protect the front faces of the chips, a silica-filled epoxy was flowed between the chips and allowed to harden, as shown in the middle pictorial of Fig. 1. This was done by depositing a bead of the epoxy on the side of the GaAs substrate using a optical fiber manipulated by a precision stage. The epoxy then wicked neatly between the chips. The chip is heated to 100 °C to reduce the viscosity of the epoxy so that it flows between the chips more easily. It is possible to meter the amount of epoxy so that it just fills the volume between chips. The epoxy is then cured by baking the chip at 100 °C for one hour. Epoxies have been used previously in this manner in flip-chip bonded assemblies to provide hermetic sealing and increase robustness [9]. For those applications the epoxy is termed an encapsulant, or underfill. Here we call it an interchip flowable hardener, to express the added function of providing a surface between the chips that is impenetrable by the substrate etch. The epoxy can be removed after substrate removal by applying a dry plasma etch using 5:1 O_2:CF_4 flow rates.

In these devices, a Ti–Au pad, place next to the n ohmic contact, is used as an integral reflector. We have previously demonstrated that modulators such as these using pure Au pads have performance equal to the best monolithic GaAs modulators [10]. Here the Ti was added to provide better sticking of the Au and so improve yield. Unfortunately our Ti–Au only has about 40% reflectivity, so the modulators here have marginal performance. We are developing schemes to use pure Au reflectors with good adhesion.

We have fabricated CMOS chips with switching node electronics (Fig. 2). Results on the switching nodes will be discussed in a later paper. Here we discuss device performance, consisting of three tests: n-ohmic bond test arrays, LED device test arrays (forward-biased modulators), and simple circuits (near bottom, Fig. 2; inset, Fig. 6). Our n-ohmic bond testers consisted of daisy-chains of devices with only n-contacts. For these we obtained 99.94% bond yield for 15×15 micron solder pads (Table I). However, our LED test arrays had only 95% device yield (Fig. 4). We have attributed this to an observable intermetallic reaction that occurs between the solder and the p-type metal during solder reflow (melting), which is shown in Fig. 6. This reaction is visible in about half the devices

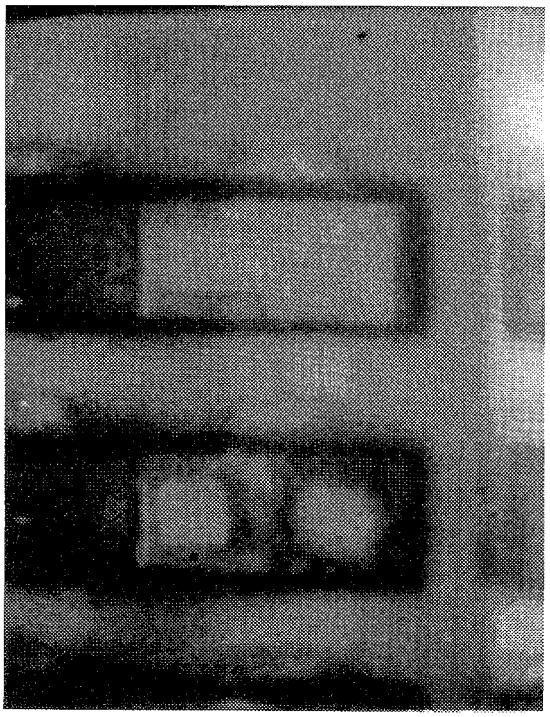

Fig. 5. Two bonded devices viewed through substrate with infrared microscope. The "tab"-shaped metal is the p-ohmic contact. The device on the left shows no degradation. The device on the right shows a reaction with the solder. There is a strong correlation with this observation and a failed device. We are examining methods of bonding without reflow to avoid this effect.

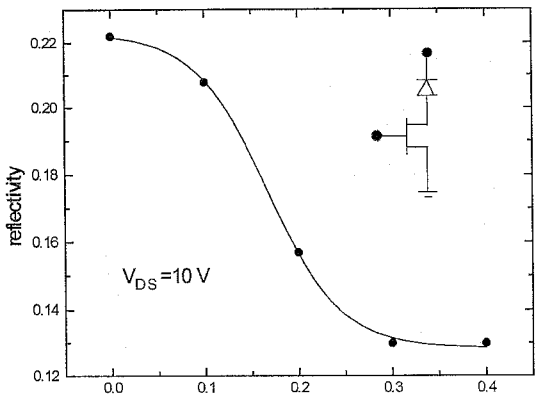

Fig. 6. Reflectivity of modulator in inset circuit versus gate-source voltage, showing electrical integration. Modulation is degraded compared to earlier devices using Au as a reflector (here Ti–Au is used).

with an infrared microscope. We have measured that if an LED is dark, there is a 96% probability that it also exhibits the intermetallic reaction. The reaction could be avoided by not performing reflow. However, it is during reflow, which is performed in a solder flux, when the solder oxide is removed. We have attempted bonding without reflow, by subjecting the chips to a plasma before bonding to remove the oxide. We have obtained sections of arrays as large as 12×42 with uniform illumination of all devices, but the results are still incomplete.

Finally, we show here a simple CMOS-modulator circuit (inset, Fig. 6). This circuit is shown on the bottom of the photo in Fig. 2. By charging the gate of the transistor, the transistor turns on and the modulator is biased. In Fig. 6 we show the turn-on characteristic. The design gate threshold of this transistor is about one volt. The turn-on of the modulator at 200 mV is consistent with this since the modulator had only nanowatts of optical power on it, so required only subthreshold operation of the transistor.

TABLE I
YIELD OF ARRAYS OF GaAs DEVICES WITH TWO n-OHMIC CONTACTS SOLDER-BONDED TO SILICON

pad size (microns)	array size	bond yield
10x10	32x80	99.88 %
15x15	28x60	99.94 %
20x20	24x50	100 %

II. CONCLUSION

We have demonstrated a practical method of integrating GaAs modulators onto silicon circuits via flip-chip bonding, followed by substrate removal. We obtain 95% device yield, and indicate that this can improve to 99.9%. We have demonstrated a simple transistor-modulator circuit to prove viability. More complex circuits will be reported at a later date.

REFERENCES

[1] A. L. Lentine, R. A. Novotny, T. J. Cloonan, L. M. F. Chirovsky, L. A. D'Asaro, G. Livescu, S. Hui, M. W. Focht, J. M. Freund, G. D. Guth, R. E. Leibenguth, K. G. Glogovsky, and T. K. Woodward, "4×4 arrays of FET-SEED embedded control 2×1 optoelectronic switching nodes with electrical fan-out," *IEEE Photon. Technol. Lett.*, vol. 6, p. 1126, 1994.

[2] J. Wieland, H. Melchior, M. Q. Kearley, C. Morris, A. J. Moseley, M. G. Goodwin, and R. C. Goodfellow, "Optical receiver array in silicon bipolar technology with self-aligned, low parasitic III/V detectors for DC-1 Gbit/s parallel links," *Electron. Lett.*, vol. 27, p. 2211, 1991.

[3] A. L. Lentine, F. B. McCormick, R. A. Novotny, L. M. F. Chirovsky, L. A. D'Asaro, R. F. Kopf, J. M. Kuo, and G. D. Boyd, "A two kbit array of symmetric self-electro-optic effect devices," *IEEE Photon. Technol. Lett.*, vol. 2, p. 51, 1990.

[4] K. W. Goossen, M. B. Santos, J. E. Cunningham, and W. Y. Jan, "Independence of absorption coefficient-linewidth product to material system for multiple quantum wells with excitons from 850 nm to 1064 nm," *IEEE Photon. Technol. Lett.*, vol. 5, p. 1392, 1993.

[5] R. N. Pathak, K. W. Goossen, J. E. Cunningham, and W. Y. Jan, "InGaAs–InP p-i(MQW)-n surface normal electroabsorption modulators exhibiting better than 8:1 contrast ratio for 1.55 μm applications grown by gas-source MBE," *IEEE Photon. Technol. Lett.*, vol. 6, no 12, pp. 1439–1441, 1994.

[6] K. W. Goossen, J. E. Cunningham, and W. Y. Jan, "GaAs 850 nm modulators solder-bonded to silicon," *IEEE Photon. Technol. Lett.*, vol. 5, p. 776, 1993.

[7] C. Camperi-Ginestet, M. Hargis, N. Jokerst, and M. Allen, "Alignable epitaxial liftoff of GaAs materials with selective deposition using polyimide diaphragms," *IEEE Photon. Technol. Lett.*, vol. 3, p. 1123, 1991.

[8] L. A. D'Asaro, L. M. F. Chirovsky, E. J. Laskowski, S. S. Pei, T. K. Woodward, A. L. Lentine, R. E. Leibenguth, M. W. Focht, J. M. Freund, G. G. Guth, and L. E. Smith, "Batch fabrication and operation of GaAs–AlGaAs field-effect transistor-self-electro-optic effect device (FET-SEED) smart pixel arrays," *IEEE J. Quantum Electron.*, vol. 29, p. 670, 1993.

[9] G. O'Malley, J. Giesler, and S. Machuga, "The importance of material selection for flip chip on board assemblies," *IEEE Trans. Components, Hybrids, Manufacturing Technol.*, part B, vol. 17, p. 248, 1994.

[10] K. W. Goossen, "Integration of GaAs modulators to silicon IC's by monolithic and hybrid techniques," in *Proc. 1994 IEEE Sarnoff Symposium*, section IIc.