A 40-GHz-Bandwidth, 4-Bit, Time-Interleaved A/D Converter Using Photoconductive Sampling

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***Abstract*—GaAs photoconductive switches have been integrated with two parallel 4-bit CMOS analog-to-digital (A/D) converter channels to demonstrate the time-interleaved sampling of wideband signals. The picosecond sampling aperture provided by low-temperature-grown-GaAs metal-semiconductor-metal switches, in combination with low-jitter short-pulse lasers, enables the optically-triggered sampling of electrical signals with tens of gigahertz bandwidth at low to medium resolution. A pair of parallel sampling paths, one for sampling and the second for feedthrough cancellation, generate a differential held signal that is quantized by a low-input capacitance, high-speed flash A/D converter. Dynamic offset averaging is employed to improve converter linearity. An experimental time-interleaved two-channel A/D converter provides about 3.5 effective bits of resolution for inputs up to 40 GHz when tested at an optically-triggered sampling rate of 160 MHz. The sampling rate was limited by the available optical source. Each A/D converter channel operates up to a 640-MHz conversion rate, dissipates 70 mW of power, and occupies an area of $150\ \mu\text{m} \times 450\ \mu\text{m}$ in a 2.5-V, 0.25-μm CMOS technology.**

***Index Terms*—Analog-to-digital (A/D) conversion, CMOS analog integrated circuits, flash converter, low-temperature-grown GaAs, metal-semiconductor-metal (MSM) devices, offset averaging, optical data processing, resistor averaging network, sample and hold, transconductance amplifiers.**

I. Introduction

HIGH-SPEED analog-to-digital (A/D) converters capable of digitizing signals with bandwidths of several tens of gigahertz have applications in optical communications, wideband radar, and high-speed instrumentation. In fiber-optic communications, dispersion effects that limit the length of the fiber link may be corrected with digital equalization techniques if A/D converters capable of conversion rates as high as 10–40 GHz are available [1]. Test instruments, such as wideband digitizing oscilloscopes, continually demand A/D converters with increased sampling rates and greater input bandwidth. Although the time interleaving of many parallel electronic A/D converters can enable very high aggregate conversion rates [2], the effective resolution of the converter at high input frequencies remains limited by the bandwidth and aperture jitter of the input sample-and-hold circuit. As illustrated in Fig. 1, the effective number of bits (ENOB) of resolution that can be achieved for a given rms aperture jitter decreases logarithmically with input frequency. Aperture jitter in the 0.5–2-ps range is typical for high-performance electronic A/D converters [3], whereas an aperture jitter of less than 0.2 ps is needed to achieve 4 effective bits of resolution at a 40-GHz input frequency.

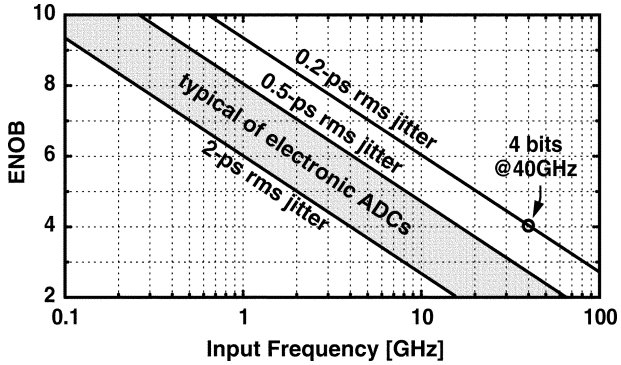

Fig. 1. ENOB of resolution versus input frequency, for varying aperture jitter.

A number of photonic sampling techniques have been proposed to overcome the limited input bandwidth and timing jitter of electronic sampling circuits [4]. These photonic techniques are enabled by mode-locked laser technology that is capable of generating periodic optical pulses with subpicosecond pulse widths and timing jitter of tens of femtoseconds. Many of the proposed photonic A/D converters involve modulating a short-pulse optical source with the input electrical signal and optically demultiplexing the modulated pulses to a number of parallel photodetectors and electronic A/D converters. The design of these systems is complicated by the need to optically demultiplex to a large number of channels in order to achieve a high aggregate sampling rate. Alternative approaches to photonic A/D conversion, such as the one proposed herein, involve sampling the electrical input with a number of parallel photoconductors that are optically triggered in sequence by time-interleaved optical pulses. Photoconductive switches with picosecond response times enable a wide input bandwidth, but generally provide poor isolation between the input and sampled signal due to capacitive coupling.

This paper introduces a parallel A/D conversion architecture, shown in Fig. 2, wherein a large number of time-interleaved photonic sampling channels each feed a 4-bit CMOS A/D converter. Integration of the photonic sampling switches with the CMOS A/D converter circuitry allows for the small hold capacitance needed to achieve a sufficiently large sample-and-hold

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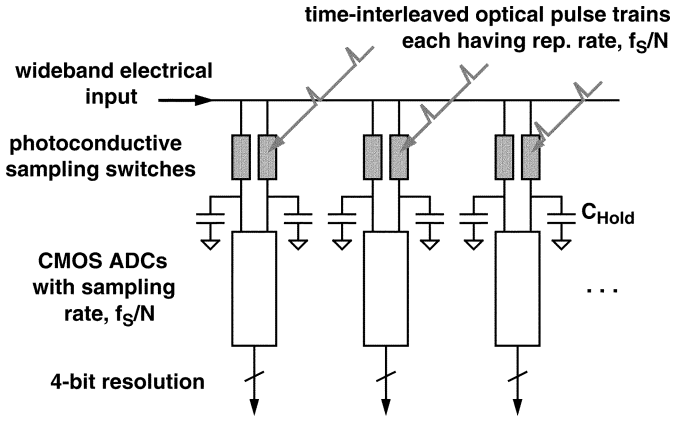

Fig. 2. Proposed time-interleaved photonic A/D converter architecture with per-channel sampling rate f_S/N, where f_S is the aggregate sampling rate and N is the number of channels.

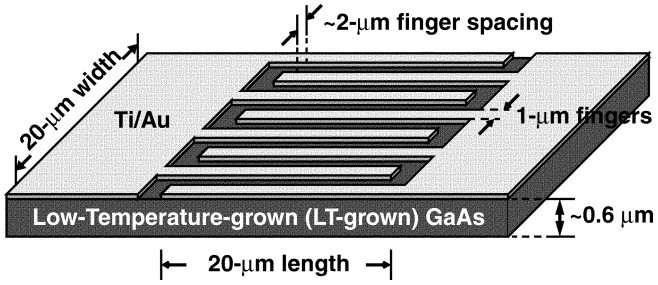

Fig. 3. Photoconductive sampling switch consisting of an 8-finger, $20\,\mu$m $\times$ $20\,\mu$m area, interdigitated MSM structure.

output voltage. Section II describes the photonic sampling technique that uses optically-triggered, low-temperature (LT)-grown GaAs switches [5] to achieve an input bandwidth of more than 40 GHz. The proposed A/D converter architecture and circuit implementation are detailed in Section III and IV. Constraints imposed by the photonic sampling switches dictate trade-offs among the input capacitance, linearity, common-mode rejection, sampling rate and resolution of the A/D converters. Additional considerations of circuit area and power ultimately led to a compact, high-speed 4-bit flash A/D converter design. An experimental prototype two-channel A/D converter was fabricated in a 2.5-V, 0.25-μm CMOS technology and integrated with LT-grown GaAs switches using a flip-chip bonding technique. Each A/D converter channel occupies an area of $150\ \mu$m $\times$ $450\ \mu$m and dissipates 70 mW at a sampling rate of 640 MHz. The prototype provides 3.5 effective bits of resolution across a 40-GHz input frequency range, at an optically-triggered sampling rate of 160 MHz. Section V describes the experimental test setup and summarizes the measured performance.

II. Photonic Sampling

The proposed photonic sample-and-hold is comprised of a LT-grown GaAs metal-semiconductor-metal (MSM) switch that is optically triggered to sample an electrical input signal onto a small hold capacitance [6]. The switch is fabricated by molecular beam epitaxy of GaAs on a semi-insulating GaAs wafer at the relatively low substrate temperature of 250°C,

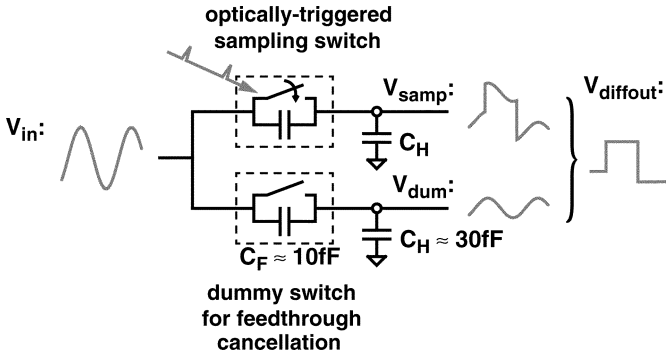

Fig. 4. Optically-triggered sample-and-hold with a replica dummy switch for feedthrough cancellation.

followed by a 1-min, 700°C rapid thermal anneal. The low epitaxial growth temperature and subsequent anneal lead to the incorporation of excess As atoms in the GaAs crystal lattice, resulting in a material with short carrier lifetimes of only a few picoseconds and high resistivity except when illuminated [5]. A titanium/gold contact metal is deposited on the LT-grown GaAs and patterned to form an interdigitated 8-finger, 2-μm finger-spacing MSM device, as illustrated in Fig. 3. The $20\,\mu$m $\times$ $20\,\mu$m area of the MSM switch is roughly equal to the spot size of the illuminating optical beam. For integration with the CMOS A/D converter circuits, the MSM switch is attached to the CMOS chip using flip-chip bonding, and the GaAs substrate is subsequently etched away to allow back-side illumination of the MSM switch. The output of the switch drives a hold capacitance, C_H, of approximately 30 fF that is composed entirely of parasitic capacitance associated with the flip-chip bonding pad and the CMOS A/D converter input. Such a small hold capacitance is necessary because of the limited drive capability of the photoconductive switch.

Sampling of the electrical input is optically triggered with a mode-locked laser generating 150-fs wide optical pulses. The incident light is absorbed in the LT-grown GaAs, thus generating excess electron-hole pairs that enable conduction between the terminals of the switch. These carriers are trapped within a few picoseconds after the light is removed, providing a very fast switch turn-off. Electrooptic-sampling measurements of the impulse response of these types of MSM switches demonstrate a 1.5-ps full-width half-maximum (FWHM) output signal [6]. Owing to its single-crystal structure, LT-grown GaAs also exhibits reasonably high carrier mobility, which helps reduce the on-resistance of the switch. The switch provides an on-resistance of $R_{\rm ON} < 100\ \Omega$ and an off-resistance of $R_{\rm OFF} > 100\ \rm M\Omega$. However, it exhibits a relatively large feedthrough capacitance, C_f, of approximately 10 fF. As a result, a large feedthrough signal is superimposed on the held voltage when the switch is in the off state.

Shown in Fig. 4 is the schematic of an optically-triggered sample-and-hold circuit employing replica feedthrough cancellation. The electrical input signal is sampled using a pair of MSM switches, of which only one is optically triggered to sample the input signal onto the hold capacitance. The second (dummy) switch provides a replica of the feedthrough signal that is subsequently subtracted from the sampled signal at

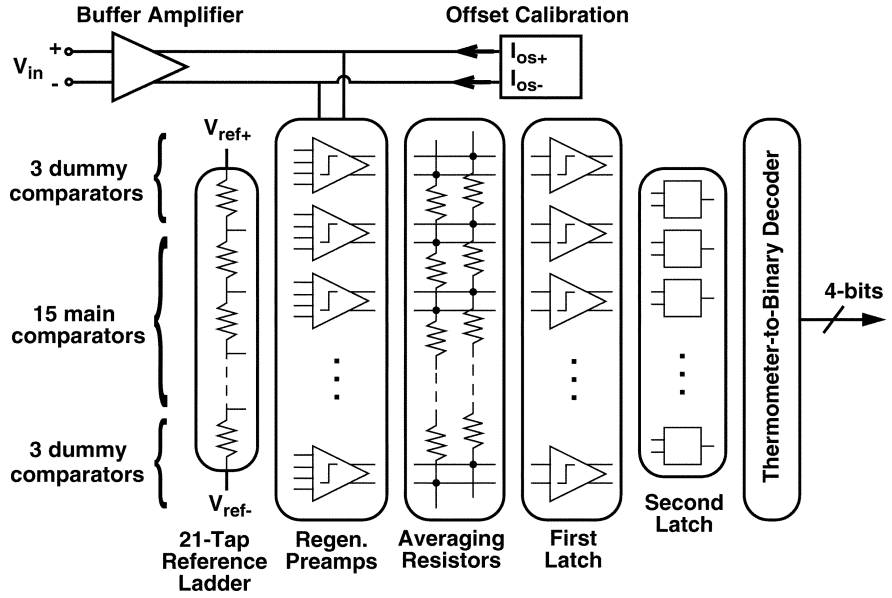

Fig. 5. Block diagram of the CMOS A/D converter.

the differential input of the CMOS A/D converter. To avoid hysteresis (memory of the previous sample), the optically sampled output, $V_{\rm samp}$, is reset by the CMOS input circuit prior to sampling, as explained in Section IV-A.

If it is assumed that the input is optically sampled at time, T_k, the differential output of the sample-and-hold circuit is

$$V_{\rm diffout}(t) = V_{\rm samp}(t) - V_{\rm dum}(t) = (1-f)\cdot V_{\rm in}(T_k) \quad (1)$$

where f is the capacitive feedthrough ratio

$$f = \frac{C_f}{C_f + C_H}. \quad (2)$$

Capacitive feedthrough is effectively eliminated at the cost of reduced output amplitude. In practice, mismatch between the two MSM switches as well as between the hold capacitances, limits the degree of feedthrough cancellation and may ultimately limit the resolution that can be achieved. The switches used in this work achieve sufficient matching for 4-bit resolution with typically less than 2% residual feedthrough in the differential output.

The finite $R_{\rm OFF}$ of the dummy MSM switch in parallel with C_f and in series with C_H forms a low-pass filter that passes the dc input voltage level to the dummy output, $V_{\rm dum}$, but also limits operation of the sample-and-hold to input frequencies well above $1/(2\pi R_{\rm OFF}C_f)$. At lower input frequencies, the switch feedthrough is no longer predominantly capacitive and the resistive feedthrough of the dummy switch attenuates the differential output signal.

III. Time-Interleaved Photonic A/D Converter Architecture

The photonic sample-and-hold circuit described in the previous section is capable of operating at sampling rates of tens of gigahertz. However, it is difficult to design a single-path A/D converter capable of digitizing the held sample at these rates. Alternatively, a highly parallel photonic A/D converter architecture, shown in Fig. 2, is proposed wherein an electrical input is sampled by a large number of time-interleaved channels to achieve a high aggregate sampling rate, f_S. Each channel consists of an optically-triggered MSM sample-and-hold circuit feeding a 4-bit CMOS A/D converter operating at a per-channel sampling rate, f_S/N, where N is the number of time-interleaved channels. The output of a mode-locked laser generating sub-picosecond wide pulses with repetition rate, f_S/N, is split into N beams, each with a different time delay, to drive the time-interleaved photonic sampling switches in succession. The optical pulses can be time-interleaved using free-space optics by introducing appropriate delay paths for each beam without significant attenuation or dispersion of the optical pulse. In free space, a 1-ps delay corresponds to an optical path length of 300 μm. Path length differences can be controlled to within a few microns, corresponding to timing skews of less than 10 fs. The use of optically-triggered sampling and time-interleaving greatly relaxes the jitter and timing skew requirements for the electrical clock signals driving the CMOS A/D converters, as well as the input bandwidth required of these converters.

The CMOS A/D converter used to digitize the sampled signals in the proposed system is constrained by the need for a very low input capacitance, as well as the low power dissipation and small area that are needed to allow the integration of many converters on a single chip. Achieving more than 6 to 8 bits of resolution is unlikely with this photonic sampling architecture because of mismatch in the replica-based feedthrough cancellation. For resolutions below 8 bits, flash A/D converter architectures generally provide the highest sampling rate per unit of power dissipated, as well as the highest sampling rate per unit area. However, the input capacitance, power, and area of a flash A/D converter scale exponentially with resolution. Another factor influencing the CMOS A/D converter design is time-interleaving errors [7] such as gain and offset mismatch among the parallel paths, which can generate objectionable tones in the output spectrum. Given these constraints, a 4-bit resolution, 640-MSample/s CMOS A/D converter was chosen

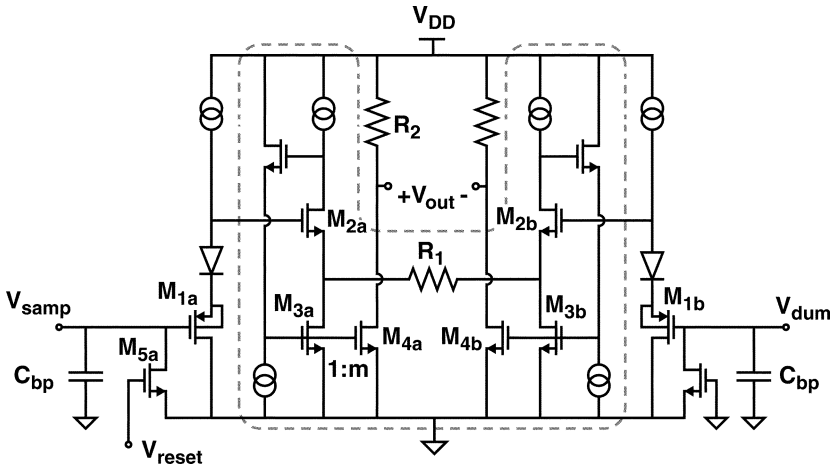

Fig. 6. Input buffer amplifier consisting of PMOS source followers driving a differential transconductor (enclosed in dashed lines).

as the vehicle for exploring the use of photonic sampling to achieve very high sampling rates and input bandwidths. Higher resolution may be possible, but the A/D converters would then likely operate at lower sampling rates and consume more power and chip area, thus limiting the number of channels that could be integrated on a single chip.

IV. Circuit Design and Implementation

Shown in Fig. 5 is a block diagram of the CMOS A/D converter. The outputs of the photonic sample-and-hold are fed to a differential buffer amplifier that subtracts the feedthrough from the held sample and provides a differential voltage gain of 4. The buffer amplifier drives a flash quantizer with a full-scale input range of 1.6 V_{pp} differential. An externally adjustable current source is used to calibrate any offset in the buffer amplifier output. The quantizer consists of 15 main comparators with an additional six dummy comparators for offset averaging.

In each comparator, a regenerative preamplifier compares the differential input against differential reference voltages generated using a resistor ladder network. The preamplifier outputs are fed to an averaging resistor network that reduces the effects of random preamplifier offsets [8]. A low-offset, low-swing first latch followed by a dynamic latch amplify the preamplifier outputs to CMOS voltage levels, thus producing a thermometer output code. CMOS logic and a 4-bit ROM decode the thermometer code to binary.

The maximum sampling rate of the CMOS A/D converter is limited by the sum of the input reset time, the buffer amplifier output settling time and the aperture time of the quantizer. For a 640-MHz sampling rate, about 250 ps of the 1.5-ns cycle time is allotted to resetting the input, 1 ns to buffer amplifier settling, and another 250 ps to comparator aperture time.

A. Input Buffer Amplifier

The input buffer amplifier has two primary constraints. First, it must amplify the differential held signal and reject the large input common-mode variation that results from the replica-based feedthrough cancellation method. Second, the buffer amplifier must present a low capacitance to the photonic sampling circuit while driving the large load capacitance of the flash quantizer. The very fast rise time of the optically sampled input also necessitates an input structure that minimizes kickback, or at least ensures any kickback is a linear function of the sampled input. In addition, the high per-channel sampling rate motivated a linearized open-loop amplifier design to minimize settling time while providing greater than 5 bits of linearity for a full-scale output.

Shown in Fig. 6, is a schematic of the input buffer amplifier together with the parasitic bond-pad hold capacitance. Both the sampled and dummy input signals are first buffered by PMOS source followers, M_{1a} and M_{1b}, with series diodes used for voltage level-shifting. Next, a differential transconductance amplifier [9], shown within the dashed lines, rejects input common-mode while providing a fixed voltage gain, A_V, set by resistor and transistor ratios. Local feedback forces a constant current in the NMOS input transistors, M_{2a} and M_{2b}, of the transconductor through control of the tail current sources, M_{3a} and M_{3b}, respectively. Neglecting the body-effect and channel-length modulation, the buffer amplifier provides a voltage gain

$$A_V = 2 \cdot m \cdot \frac{R_2}{R_1} \tag{3}$$

where m is the ratio of the width of NMOS current sources, M_{4a} and M_{3a}.

An important concern in the buffer amplifier design is kickback to the dynamically held input voltage. The optically sampled input has a fast rising/falling edge of less than a few picoseconds. During this transient, the output of the PMOS source follower, M_{1a}, remains approximately constant, so the input charges both its gate-to-source and gate-to-drain capacitances, C_{gs} and C_{gd}. As the PMOS source follower settles, its output is coupled back to the input through C_{gs}. The amount of charge kicked back to the input depends on the magnitude of C_{gs} and the difference between the sampled input voltage and the previous held voltage. To minimize distortion from nonlinear C_{gs}, the input signal amplitude is kept small and the PMOS source follower is biased with a sufficiently large overdrive voltage $V_{gs} - V_{th}$, to ensure that the charge kickback is a relatively linear function of the sampled input voltage. To avoid memory of the previous sample, the sampled input is reset to ground with

NMOS transistor M_{5a}, prior to optical sampling. The dummy input is not reset because its dc voltage-level is determined by MSM switch leakage; resetting would add a signal-dependent offset.

Relatively small PMOS input transistors are used in order to meet the low input capacitance requirement. However, both mismatch in threshold voltage $V_{\rm th}$ and device transconductance $\beta = \mu C_{\rm ox} W/L$ increase with $1/\sqrt{(W \cdot L)}$ [10]. As a result, mismatch between the PMOS input devices is the dominant source of offset in the buffer amplifier. Implementation of any real-time offset correction circuits is difficult without introducing significant input capacitance. Therefore, offset is corrected at startup (to within a few millivolts) by adding a manually adjusted current source to the buffer amplifier output. The main source of buffer amplifier gain error is β-mismatch in the NMOS current source transistors. These devices, being large in size, provide sufficient matching to achieve a 1-sigma gain variation of less than 1.5%.

The input voltage range of the buffer amplifier was chosen primarily on the basis of linearity constraints. A larger input voltage swing would require less amplifier gain and less settling time, but would degrade the linearity. In particular, second harmonic distortion from the large input common-mode variation is the main source of nonlinearity in the buffer amplifier response. The buffer was designed to provide a nominal voltage gain of 4, and about 6 bits of linearity when sampling a 0.56 $V_{\rm pp}$ input to the A/D converter. Due to capacitive feedthrough, the input to the buffer is a 0.4 $V_{\rm pp}$ differential held signal with a common-mode variation of 0.35 $V_{\rm pp}$. Based on HSPICE simulations with the quantizer loading the outputs, the buffer amplifier achieves a slightly underdamped step response with a 3-dB bandwidth of 1.5-GHz and consumes about 22 mW of power for typical process parameters.

B. Regenerative Preamplifier

The aperture time, input capacitance and linearity of the flash quantizer are determined primarily by the preamplifier circuit. The main function of the preamplifier is to provide sufficient gain to overcome the offset of the subsequent comparator without introducing significant offset of its own. However, a short aperture time and low input capacitance are also necessary to ease the settling time requirements of the preceding buffer amplifier. A high-gain preamplifier generally has less bandwidth and requires a longer aperture time over which the input must remain stable. Random offsets due to transistor mismatch, which is the main source of quantizer nonlinearity, may be improved by increasing device dimensions at the expense of higher input capacitance.

In an A/D converter with a front-end sample-and-hold circuit, a large preamplifier bandwidth is desirable to track the sampled input as it settles, whereas high gain is desirable once the input has settled. The regenerative preamplifier circuit shown in Fig. 7 uses an output reset switch, M_0, to prevent regeneration and provide a high output bandwidth while the input is settling. Releasing the reset switch allows the cross-coupled PMOS transistors, M_1 and M_2, to regenerate the output, providing high gain in a short amount of time. The offset of the regenerative preamplifier is comparable to that of a preamplifier with diode-connected PMOS load transistors. However, regeneration provides for much higher gain. The output of the preamplifier is limited in amplitude by the loading of the averaging resistor network; otherwise, the outputs would regenerate to full-scale.

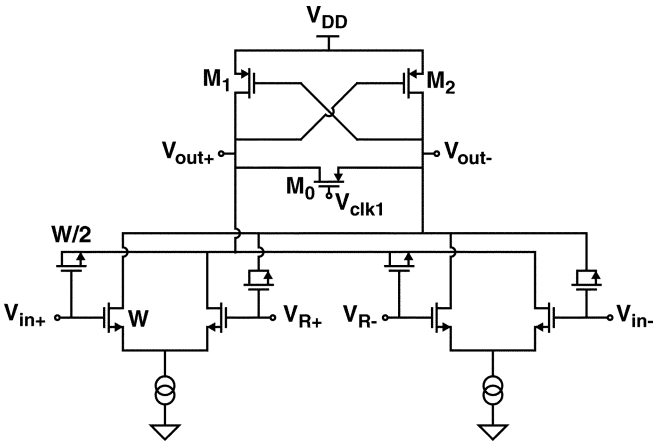

Fig. 7. Regenerative preamplifier with reset switch M_0 and capacitive feedback cancellation.

During the regeneration phase, cross-connected MOS capacitors cancel differential feedback through the gate-to-drain overlap capacitance that may otherwise distort the input. These MOS capacitors are operated below threshold to more accurately duplicate the overlap capacitance.

C. Averaging Resistor Network

Resistive output offset averaging is used to reduce quantizer nonlinearity and relax device matching constraints in the preamplifier circuit [8]. With averaging, much smaller preamplifier device dimensions may be used to achieve a given level of offset error, with a corresponding large reduction in input capacitance and power dissipation. The offset reduction obtained with an averaging resistor network is largely dependent on the output load resistance of the preamplifier circuit. Kattmann and Barrow [8] show that for a resistive load, R_L, the improvement in differential nonlinearity (DNL) is maximized by increasing the ratio of $R_L/R_{\rm avg}$, where $R_{\rm avg}$ is the averaging resistance. Bult and Buchwald [11] attempt to maximize the amount of averaging benefit by using an effectively infinite R_L constructed from parallel diode-connected and cross-coupled PMOS loads whose positive and negative small-signal conductances cancel each other. Averaging can provide similar offset reduction in arrays of regenerative preamplifiers that have a *negative* net load resistance and provide significantly higher gain. With regenerative preamplification, the output must be first reset and the offset averaging occurs dynamically. A similar combination of regeneration and averaging are employed by Choi and Abidi [12] in their first-stage latch.

Shown in Fig. 8 is a schematic of the preamplifier array with the output averaging resistor network. In addition to the 15 main preamplifiers, overrange dummy preamplifiers have been added to avoid any discontinuity in the averaging at the edges of the main array. Each preamplifier is active over an input range of ± 3 LSB, so that three overrange preamplifiers are needed at each end of the main array to ensure the first and last overrange preamplifiers are always operating near saturation for full-scale

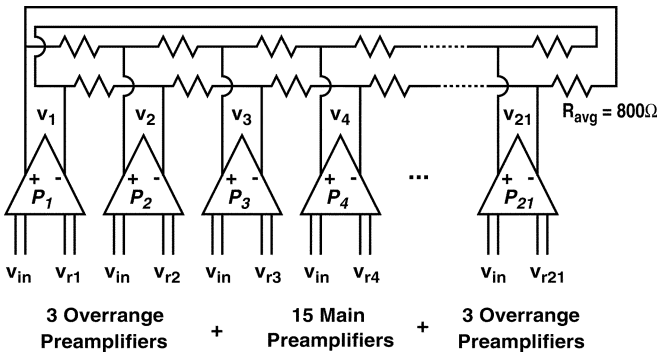

Fig. 8. Implementation of resistive offset averaging of preamplifier array outputs.

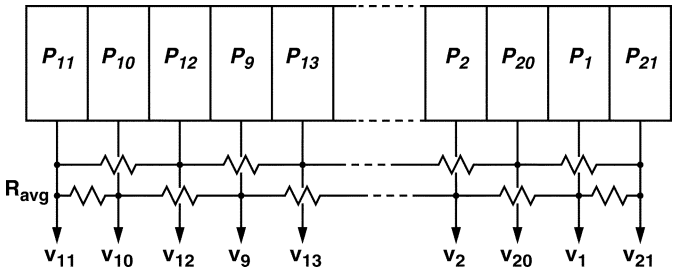

Fig. 9. Layout of preamplifier array with averaging resistor network (for simplicity, only single-ended outputs are shown).

inputs. The complementary outputs of the first and last overrange preamplifiers are cross-connected through a pair of averaging resistors so that every preamplifier in the array sees the same effective load impedance and has a balanced number of preamplifiers contributing to its output.

In general, the added overrange preamplifiers reduce the input range available to the main preamplifier array, thus reducing the maximum quantization step size that can be used. However, in this design the linearity of the buffer amplifier already limits the quantization step size, so the input range of the main preamplifier array is unaffected by the presence of overrange preamplifiers. The addition of the overrange preamplifiers does increase the input capacitance and power dissipation. Ref. [13] suggests an averaging termination technique that may be used to reduce the number of overrange amplifiers in a conventional resistor-loaded preamplifier array, but the approach is difficult to apply to a regenerative implementation.

If the preamplifier array shown schematically in Fig. 8 was laid out sequentially, a pair of long interconnects would be needed to connect the ends of the preamplifier array. To avoid the large parasitic capacitance and resistance that would be introduced by such an interconnect, the preamplifier array is laid out in a single interleaved row as shown in Fig. 9. With this layout pattern, all adjacent preamplifiers (e.g. P_k and P_{k+1}) are at most 2 cell widths apart.

The value of $R_{\rm avg}$ was chosen to minimize the net input-referred offset, $\sigma_{\rm os,total}$, due to preamplifier offset, $\sigma_{\rm os,pa}$, and offset in the subsequent comparator, $\sigma_{\rm os,comp}$. A small $R_{\rm avg}$ improves averaging of preamplifier offsets at the expense of less preamplifier gain, G_{pa}, resulting in a greater input-referred

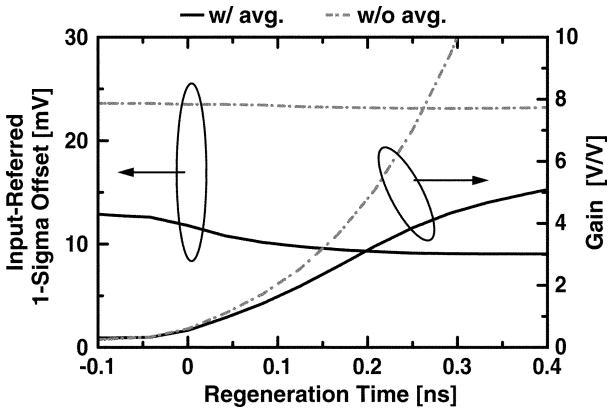

Fig. 10. Simulated preamplifier offset and gain versus regeneration time with and without resistor averaging.

offset contribution from the comparator. If the preamplifier and comparator offsets are independent random variables, then

$$\sigma_{\rm os,total} = \sqrt{\sigma^2_{\rm os,pa}(R_{\rm avg}) + \left(\frac{\sigma_{\rm os,comp}}{G_{pa}(R_{\rm avg})}\right)^2} \qquad (4)$$

Fig. 10 shows the results of Monte Carlo simulations of the preamplifier offset and gain as functions of regeneration time, without averaging and with $R_{\rm avg} = 800\ \Omega$. The time at which the clock signal crosses $V_{DD}/2$ is defined as $t = 0$. Without averaging, the preamplifier offset remains constant and the gain increases exponentially, as expected. However, with averaging, the preamplifier input-referred offset is greatly reduced and decreases further as the output regenerates, but gain is also reduced because the averaging resistors load the outputs. In the reset phase, the preamplifier has a differential voltage gain of about 0.3 and provides 3-GHz of bandwidth with an effective load resistance, $R_{\rm L,reset} \approx 800\ \Omega$. The low $R_{\rm L,reset}/R_{\rm avg}$ ratio results in a moderate factor of 1.8 offset reduction. During the regeneration phase, the preamplifier offset is dynamically averaged with an effective $R_{\rm L,regen} \approx -2$ kΩ. If a preamplifier output regenerates toward a voltage level that is not halfway between the outputs of the adjacent preamplifiers, then the averaging resistors pull the output back toward the middle. As the outputs grow larger, so does the current in the averaging resistor network, eventually limiting the preamplifier gain that may be obtained. After a 250-ps regeneration time, the preamplifier offset is reduced by a factor of 2.6, but the voltage gain is also reduced from 7 to 4 when compared to the preamplifiers without averaging.

D. First and Second Latch

A two-stage latch follows the preamplifier to provide additional regenerative gain. The first stage, shown in Fig. 11, is a low-offset, low-output-swing latch that is biased with a constant current. The first latch maintains a constant output common-mode level during the reset and regeneration phases, which helps to reduce any input-referred offset due to mismatch in the output capacitive loads. An NMOS transistor, M_0, clamps the output voltage swing for fast overdrive recovery. M_0 is biased in cutoff to minimize loading of the output nodes except in the presence of large output swings.

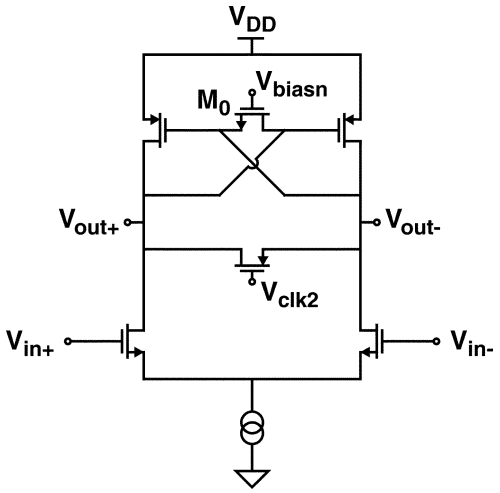

Fig. 11. First-stage low-offset latch with NMOS clamp.

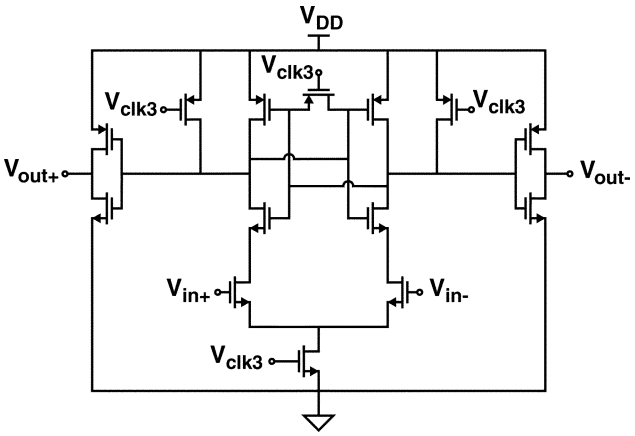

Fig. 12. Second-stage differential edge-triggered latch with CMOS output voltage levels.

The output of the first latch is fed to a second differential edge-triggered latch [14], shown in Fig. 12, that amplifies its input to CMOS voltage levels. The array of latches provide a thermometer code output that drives a 4-bit ROM to generate the corresponding binary output code.

V. Experimental Results

Shown in Fig. 13 is a die micrograph of a prototype two-channel A/D converter fabricated in a 0.25-μm CMOS technology. The LT-grown GaAs MSM switches have been integrated with the CMOS chip using flip-chip bonding. Each A/D converter channel occupies a $150\,\mu\text{m} \times 450\,\mu\text{m}$ area and consumes about 70 mW of power, not including output drivers, at a sampling rate of 640 MSample/s. The electrical input signal is driven directly onto the chip using a ground-signal-ground (G-S-G) coplanar microwave probe to avoid package parasitics and terminated on-chip with a 50-Ω polysilicon resistor. The digital outputs of the A/D converter are buffered and driven off chip using differential current-mode signaling with an off-chip termination resistance of 150 Ω. The output drivers consist of open-drain NMOS differential pairs biased with a constant tail current in order to minimize digital switching noise.

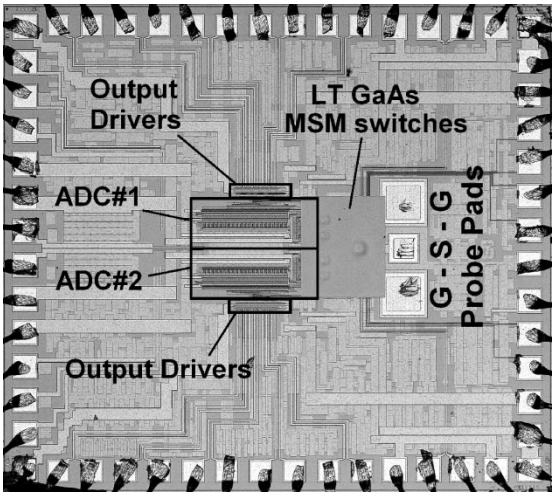

Fig. 13. Chip micrograph of prototype two-channel photonic A/D converter.

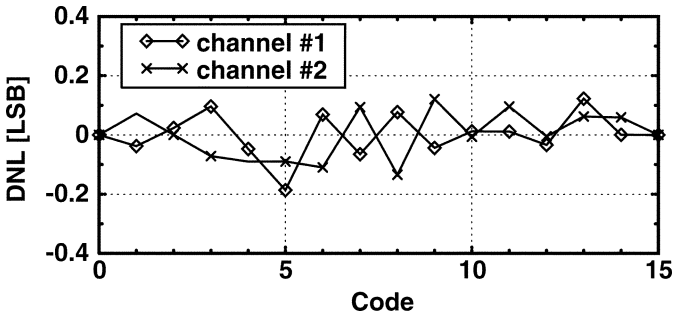

Fig. 14. Measured DNL of each CMOS A/D converter at 640 MS/s.

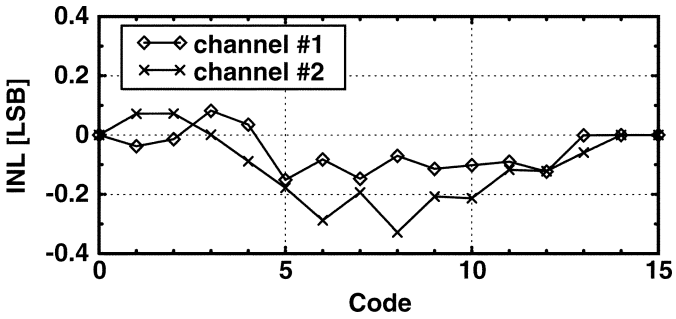

Fig. 15. Measured INL of each CMOS A/D converter at 640 MS/s.

Static mismatch between the two A/D converter channels and linearity errors in each of the channels were measured with a low-frequency signal applied directly to the CMOS A/D converter inputs through small NMOS pass-transistors. The measured gain mismatch of the two channels was 1.5%, and the offset mismatch before and after calibration were 62 mV (0.62 LSB) and <2 mV (0.02 LSB), respectively. The DNL and integral nonlinearity (INL) of each A/D channel were measured for a 2.5-MHz input signal and a 640-MHz conversion rate using the code density test [15]. As shown in Fig. 14 and Fig. 15, the prototype has a peak DNL and INL of 0.2 LSB and 0.35 LSB, respectively.

Fig. 16 illustrates the test setup used to evaluate the performance of the A/D converter with optically-triggered sampling. An 850-nm titanium/sapphire mode-locked laser generates 150-fs wide optical pulses at an 80-MHz repetition rate. The

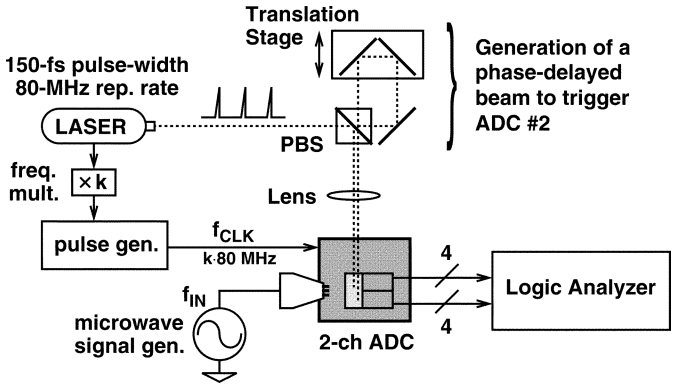

Fig. 16. Setup for testing the prototype time-interleaved two-channel A/D converter.

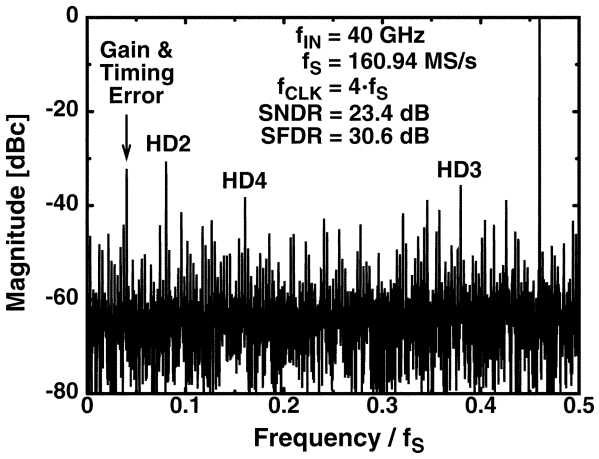

Fig. 17. Output spectrum (8192-point FFT) of the time-interleaved two-channel A/D converter with $f_S \approx 160$ MS/s and $f_{\rm IN} = 40$ GHz.

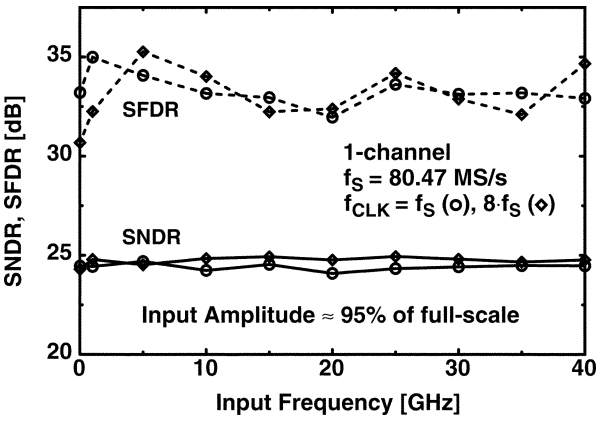

Fig. 18. Measured SNDR and SFDR versus input frequency for single-channel operation.

output of the laser is split into two beams using a polarization beam splitter (PBS). The vertical polarization is reflected by the PBS and focused onto the MSM sampling switch of A/D converter channel #1, whereas the horizontal polarization is transmitted through the PBS and appropriately delayed with mirrors and a micrometer-precision translation stage before being focused onto the MSM sampling switch of A/D converter channel #2. The relative delay of the two optical beams can be adjusted to about 6-fs precision by varying the optical path length in 2-μm steps. An optical power of about 4 mW per channel, corresponding to a pulse energy of 50 pJ, is required to activate the MSM switch and fully charge the hold capacitance. The CMOS A/D converters are driven by an electrical clock at frequency $f_{\rm CLK}$, generated with a pulse generator that is phase-locked to the laser. The pulse generator allows 1-ps delay adjustments in $f_{\rm CLK}$ that are used to align the CMOS A/D converter timing with the optical sampling pulses. A 40-GHz microwave signal generator provides the high frequency input signal and the digital outputs of the A/D converter are captured with a logic analyzer.

The test setup was limited to an optically-triggered sampling rate of 80 MHz per channel by the available laser. However, operation of the A/D converter was demonstrated at higher conversion rates by using an $f_{\rm CLK}$ that is a multiple, k, of 80 MHz. A higher $f_{\rm CLK}$ reduces the time available for quantization and stresses A/D converter operation. Since the input signal is optically sampled at an 80-MHz rate, only every kth digital output of the A/D converter is valid, and the intermediate $k-1$ outputs are discarded in software. Although scaling $f_{\rm CLK}$ demonstrates the potential for higher frequency operation, this test may fail to capture hysteresis in the A/D converter that may occur at higher optical sampling rates. However, since the sampled input to the CMOS A/D converter is reset prior to each conversion cycle, significant hysteresis is not expected.

The A/D converter's dynamic performance was evaluated by taking the fast Fourier transform (FFT) of the digital output when a single tone is applied to the input of the converter. Fig. 17 illustrates the dominant distortion tones in the output spectrum obtained by taking the 8192-point FFT of the A/D converter outputs when sampling a 40-GHz input tone at a sampling rate of $f_S \approx 160$ MS/s. Undersampling, that is sampling below the Nyquist rate, causes the input tone and all of its harmonics to alias into the Nyquist bandwidth from zero to $f_S/2$, but preserves signal, distortion, and noise power. The spurious-free dynamic range (SFDR) of the A/D converter is determined by dividing the power in the fundamental tone by the power in the largest other tone in the output spectrum, which in this case is the second harmonic, $HD2$. The signal-to-noise-plus-distortion ratio (SNDR) is calculated by dividing the power in the fundamental tone by the total baseband noise and distortion power other than that in the fundamental.

Fig. 18 shows a plot of the SNDR and SFDR measured for operation of a single channel of the A/D converter over an input frequency range from 3 MHz to 40 GHz and at a digital output amplitude of 95% of full-scale. The input to the one-channel A/D converter is optically sampled at $f_S \approx 80$ MS/s. However, the A/D converter performance was evaluated for both $f_{\rm CLK} \approx 80$ MHz and $f_{\rm CLK} \approx 640$ MHz. In both cases, the SFDR is limited to about 32 dB (5 bits) by second harmonic distortion in the input buffer amplifier, which is a consequence of the large input common-mode variation that results from capacitive feedthrough in the sampling circuit. The SNDR remains approximately constant with input frequency up to 40 GHz and does not appear to be limited by jitter from the sampling switches, the laser or the input source. The extent to which the measured baseband noise exceeds the quantization noise is assumed to be

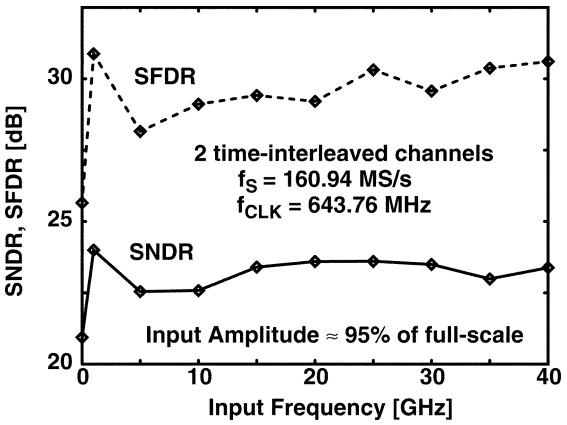

Fig. 19. Measured SNDR and SFDR versus input frequency for operation of two time-interleaved channels.

TABLE I
PERFORMANCE SUMMARY

Technology		1p5m 0.25-μm CMOS
Supply Voltage		2.5 V
A/D Conversion Rate		2×640 MHz
Optical Sampling Rate		2×80 MS/s
Nominal Resolution		4 b
Input Range		560 mV peak-to-peak
Input Bandwidth		3 MHz to 40 GHz
Peak SNDR / SFDR @f_{IN} = 40 GHz		23.4 dB / 30.6 dB
DNL / INL		0.2 LSB / 0.35 LSB
Area per chan. (excl. drivers)		150×450 μm^2
Power per channel:	Analog	40 mW @f_{CLK} = 640 MHz
	Digital (excl. drivers)	30 mW @f_{CLK} = 640 MHz
	Optical	~4 mW @f_S = 80 MS/s

the result of sampling jitter. If the quantization noise is assumed to have a uniform spectral density, then an upper bound for the sampling jitter of 80-fs can be estimated from the measured signal-to-noise-ratio (SNR). The effective resolution bandwidth of the A/D converter may be significantly higher than 40 GHz, but a higher frequency source was not available.

The measured SFDR and SNDR of the time-interleaved two-channel A/D converter are shown in Fig. 19. The SFDR is again limited by second harmonic distortion that is presumed to occur in the input buffer amplifier. SNDR does not appear to degrade with input frequency, which indicates that the performance is not limited by either sampling jitter or distortion from timing skew between the two channels.

The measured performance of the experimental prototype is summarized in Table I.

VI. CONCLUSION

An optically-triggered sample-and-hold circuit employing LT-grown GaAs MSM switches has been integrated with parallel CMOS A/D converters to demonstrate the feasibility of a wide-bandwidth, time-interleaved photonic A/D converter architecture. The MSM switches provide aperture times of a few picoseconds, with precise sampling times derived from a low-jitter, short-pulse laser. Each time-interleaved channel samples the electrical input with a pair of MSM switches, one for sampling and a second replica switch for feedthrough cancellation. The differential held signal is quantized by a high-speed CMOS A/D converter in which a low-input-capacitance buffer amplifier rejects input common-mode variations in the held signal and provides a fast-settling output to drive a 4-bit flash quantizer. Resistive offset averaging is applied to an array of regenerative preamplifiers to decrease the input capacitance and power dissipation of the flash quantizer by relaxing transistor matching constraints.

A prototype two-channel A/D converter has been implemented in a 2.5-V, 0.25-μm CMOS technology and integrated with LT-grown GaAs MSM switches using flip-chip bonding. Each A/D converter channel operates at up to a 640-MHz sampling rate, dissipates 70 mW, and occupies an area of 150 μm $\times$ 450 μm. At an optically-triggered sampling rate of 160 MS/s, the time-interleaved converter achieves greater than 3.5 effective bits of resolution at a 40-GHz input frequency with over 30 dB of SFDR and an estimated sampling jitter of less than 80 fs. The wide input bandwidth, precise timing, low area, and low power suggest the feasibility of integrating a larger number of parallel channels to achieve much higher sampling rates.

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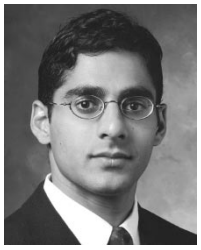

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