Low-Temperature Growth of GaAs on Si Used for Ultrafast Photoconductive Switches

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***Abstract*—GaAs was grown directly on silicon by molecular beam epitaxy (MBE) at low substrate temperature (∼250 °C). Both the silicon wafer cleaning and the GaAs film growth processes were done at temperatures lower than the Si–Al eutectic temperature to enable monolithic integration of low-temperature-GaAs photoconductive switches with finished Si-CMOS circuits. The film surfaces show less than 1 nm rms roughness and the anti-phase domain density is below the detection limit of X-ray diffraction. Metal–semiconductor–metal photoconductive switches were made using this material and were characterized using a time-resolved electrooptic sampling technique. A full-width at half-maximum switching time of ∼2 ps was achieved and the responsivity of switches made from low-temperature GaAs on Si material was comparable to its counterpart on a GaAs substrate.**

***Index Terms*—GaAs on Si, low substrate temperature, low-temperature-grown GaAs (LT-GaAs), metal–semiconductor–metal (MSM) switch, monolithic integration.**

I. Introduction

Modern communications and high-speed instrumentation require much higher speed analog-to-digital converters (ADCs) with bandwidths up to several tens of gigahertz. Conventional electronic ADCs are extremely powerful in signal processing. However, their performance at high speeds is limited by low input bandwidth and a fundamental timing jitter problem which causes aperture uncertainty. On the other hand, photonic devices have high bandwidth and superior timing accuracy advantages, although their signal processing capability is inferior to electronic devices. Therefore, a hybrid system would potentially combine the advantages of both technologies to achieve superior performance. Based on this idea, we previously proposed a CMOS/photonic analog-to-digital (A/D) conversion system utilizing a sample-and-hold scheme with low-temperature-grown GaAs (LT-GaAs) metal–semiconductor–metal (MSM) photoconductive switches. In order to achieve high input bandwidth in this system, the switches would be triggered by a femtosecond-order optical pulse to sample the input electrical signal onto a hold capacitor. Sampled data would later be digitized at a much slower rate using CMOS ADCs attached to the sample-and-hold circuit. We use a time-interleaved parallel architecture with multiple channels to achieve an ultrafast aggregate sampling rate. The details of our A/D conversion system can be found elsewhere [1], [2].

Manuscript received November 6, 2003; revised February 11, 2004. This work was supported by DARPA/PACT under Contract DAAD17-99-C-0048.

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Digital Object Identifier 10.1109/JQE.2004.828234

LT-GaAs is our choice of material for the photoconductive switches. This material is usually grown by molecular beam epitaxy (MBE) at substrate temperatures as low as 200 °C to 350 °C, compared to conventional GaAs which is grown at 550 °C–650 °C. Due to the low growth temperature, LT-GaAs is highly nonstoichiometric, with a large density of excess arsenic incorporated into the GaAs matrix, forming a high concentration of As-related deep-level defects. These defects result in an ultrashort carrier lifetime [3]. A high-temperature postgrowth anneal at above 600 °C is usually utilized to increase the carrier mobility, but not substantially increase the lifetime. The LT-GaAs material was chosen in our system because of its picosecond or subpicosecond carrier lifetime that allows for ultrafast switching, reasonably high mobility to provide good switch responsivity, as well as high dark resistivity and high breakdown field [3].

One of the key innovations of our study is the monolithic integration of high-speed LT-GaAs photoconductive switches with low-power Si CMOS integrated circuits. We have previously used a flip-chip bonding technique for integration and demonstrated a two-channel prototype ADC with ∼3.5 effective bits of resolution for an input bandwidth up to 40 GHz and an estimated total timing jitter of less than 80 fs [2], [4]. To minimize the input parasitics, monolithic integration is explored. A common approach is to finish the final level metallization of the IC after growth of the GaAs devices. However, this approach creates significant fabrication perturbation. While limited success has been achieved to make majority-carrier GaAs devices on Si [5], the material quality requirements for the ultrafast switch application are more forgiving and the low growth temperature is compatible with completely fabricated CMOS circuits. Low-temperature treatments also promise not to alter the doping profile in the underlying Si ICs and greatly reduce the thermal stress caused by the 60% difference in the thermal expansion coefficients between GaAs and Si. Therefore, we are investigating the direct growth of LT-GaAs on finished Si CMOS wafers. In our approach, the critical step is cleaning the Si wafer surface at temperatures low enough not to damage the metal interconnects and other components in Si circuits. In this paper, we present a first-step study of LT-GaAs growth on Si substrates. Growth results on real circuits will be reported later.

II. Experiments and Results

A. Wafer Cleaning and Film Growth

The LT-GaAs layers were grown on nominal (100) Si substrates and vicinal (100) Si substrates oriented 4° off toward

[011]. The substrates were chemically cleaned in a class-100 clean room, using a modified RCA cleaning method. Wafers were first immersed into a 4:1 H_2SO_4: H_2O_2 solution at 90 °C for 10 min to remove trace organics. For removal of trace metal ions, samples were submerged into a 5:1:1, H_2O : H_2O_2 : HCl solution at 70°C for 10 min. A 30-s dip in a 50:1 H_2O : HF solution was done for oxide etching. A final dip into a low-concentration HF solution was done to achieve hydrogen passivation immediately before loading the wafers into the loadlock chamber. The wafers were baked in the load chamber at 200 °C for 1 h to remove moisture and gases.

All samples were grown in a solid-source Varian Gen II MBE system. Gallium flux was supplied by a thermal effusion cell and dimeric arsenic (As_2) was provided through a valved thermal cracker. For the wafers investigated here, a ~0.5-μm-thick layer of GaAs was grown at a rate of 0.2 μm/hr with an As_2/Ga beam-equivalent-pressure (BEP) ratio of 6. *In situ* RHEED was used to monitor the surface cleaning and the surface condition at each stage of the film growth. During the heat cleaning step to desorb hydrogen, the Si surfaces typically start to exhibit a streaky 2×1 reconstruction pattern at temperatures as low as ~450 °C. Samples in this article were then subsequently baked at ~550 °C for 20 min (although the RHEED pattern at ~480 °C was almost the same as that seen at ~550 °C) and then cooled down to the growth temperature (~250 °C) with exposure to an As flux to avoid any further contamination from the chamber during the cooling process. The As flux serves both as a protection and a prelayer for the purpose of anti-phase domain (APD) suppression. The literature [6] and our experience show that the hydrogen desorption peak is ~510 °C. Thus, by holding for a longer time, this cleaning temperature could be further lowered when growing on circuits. The LT-GaAs growth was initiated with 10 migration-enhanced-epitaxy (MEE) cycles. After the MEE cycles, the RHEED pattern became dim and spotty, indicating island formation and three-dimensional (3-D) growth.

During growth, the RHEED pattern changed and the LT-GaAs layer grown on Si became 1×1, similar to LT-GaAs grown on a GaAs substrate. Upon *in situ* annealing, the RHEED patterns exhibited a streaky 2×4 reconstruction [see Fig. 1(a) and (b)], indicating a high-quality single-domain GaAs layer with a smooth surface. All samples appear specular and featureless to the naked eye and under an optical microscope after removal from the MBE system.

Following the growth, the samples were annealed at ~600 °C for 10 min either in the growth chamber under an As overpressure or in a rapid thermal annealing (RTA) chamber under N_2 ambient. During RTA annealing, the samples were covered with a protective GaAs wafer to prevent As desorption. Laser annealing techniques could be used to avoid this high-temperature anneal when growing on real CMOS chips.

B. Film Characterization

The roughness of the film surface was observed using AFM. Several 2 μm × 2 μm area scans were done. As shown in Fig. 2, for 0.5-μm-thick LT-GaAs grown on a nominal (100) Si substrate, the rms roughness was ~1.0 nm. For the same thickness LT-GaAs layer grown on a vicinal (100) Si substrate (4° miscut toward [011] direction), the rms roughness was ~0.5 nm. Section analysis showed the peak-to-peak variation across the surface was ~6 nm for the film grown on the nominal (100) substrate and ~3 nm for the misoriented substrate. This roughness is approximately an order of magnitude smaller than the best previously reported data [7].

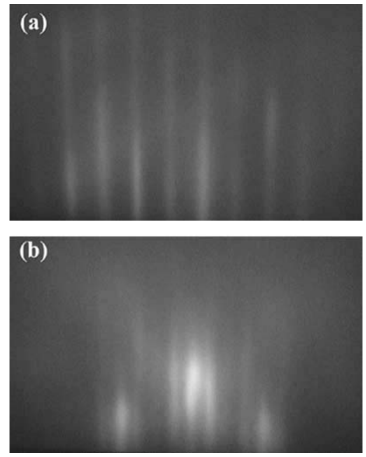

Fig. 1. RHEED patterns for LT-GaAs films grown on Si substrates and *in situ* annealed at ~600 °C for 10 min. (a) [011] azimuth. (b) $[0\bar{1}1]$ azimuth.

The film quality was studied by high-resolution (0.0001°) X-ray diffraction (XRD). The ratio between the GaAs (002) peak intensity and GaAs (004) peak intensity is comparable to that of a conventional GaAs homoepitaxy reference wafer. The full-width at half-maximums (FWHMs) of each peak for both samples are summarized in Table I. The GaAs (002) superstructure reflection is very sensitive to APDs, while the (004) fundamental reflection is not affected by APDs. To experimentally determine if APDs exist in an ordered crystal, the widths of the superstructure and fundamental reflections must be compared [8]. It is clear that, for growth on both substrates, the (002) superstructure peak is not broadened compared to the (004) fundamental peak. This indicates that the APD density is below the detection limit of XRD [8]. In addition, a decrease in the FWHM of both peaks was observed when growing on the vicinal substrate compared to the nominal substrate.

C. MSM Switch Characterization

Using this material, MSM photoconductive switches were made to characterize the mobility and carrier lifetime of LT-GaAs grown on Si substrates. Switches with an interdigitated pattern were fabricated by depositing titanium/gold contact metal on the LT-GaAs epi-layers through a standard lift-off process. Devices with different finger spacings and finger widths were patterned in a ~ 20 μm × 20 μm area, the approximate optical spot size used for characterization.

The switch was placed in the middle of a coplanar waveguide transmission-line structure for high-speed characterization, as shown in Fig. 3. The transmission-line pattern was also made by depositing titanium/gold metal on the LT-GaAs film. For the measurement, the switch was dc-biased and optically triggered by a titanium/sapphire mode-locked laser pulse with ~150 fs FWHM pulse width, ~850 nm center wavelength, and a ~80

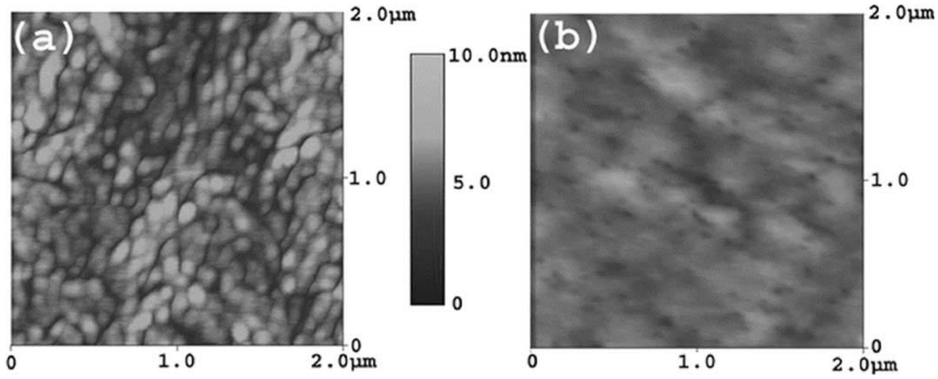

Fig. 2. 2 μm $\times$ 2 μm AFM images. (a) A 0.5-μm-thick LT-GaAs layer grown on a nominal (100) Si substrate. RMS roughness is $\sim$1.0 nm and peak-to-peak variation is $\sim$6 nm. (b) A 0.5-μm-thick LT-GaAs layer grown on a vicinal (100) Si substrate 4° misoriented toward the [011] direction. RMS roughness is $\sim$0.5 nm and peak-to-peak variation is $\sim$3 nm.

TABLE I
GaAs Peak FWHM Comparison for LT-GaAs Films Grown on Different Si Substrates

	GaAs (004) peak FWHM	GaAs (002) peak FWHM
on nominal substrate	396 arcsecs	331 arcsecs
on vicinal substrate	357 arcsecs	276 arcsecs

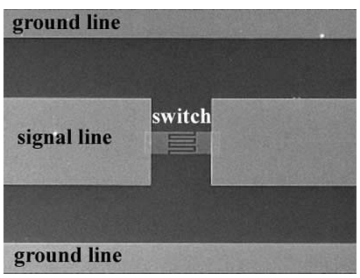

Fig. 3. SEM picture of MSM switch characterization structure.

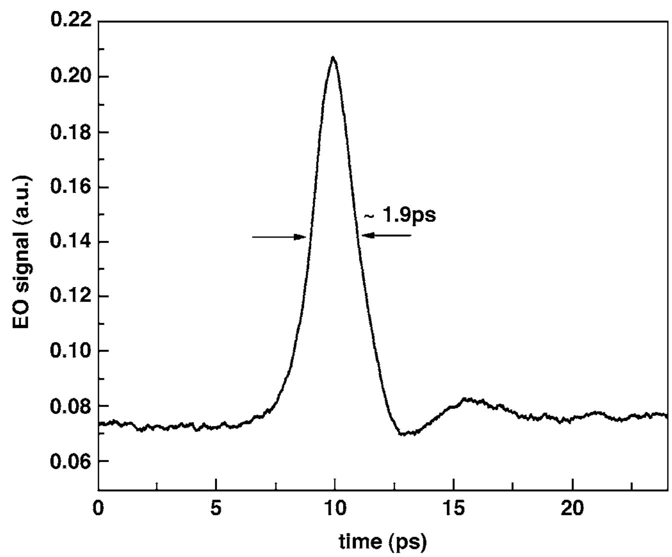

Fig. 4. Output waveform characterized using an EO sampling technique for a photoconductive MSM switch made from LT-GaAs on a vicinal (100) Si substrate. The switch has a 2-μm finger width and 1-μm finger spacing, tested under 1 mW optical power and 5 V bias voltage.

MHz repetition rate. The movement of photogenerated carriers causes an electrical transient to propagate down the transmission line. Therefore, by properly measuring this transient, the responsivity and speed of the switch can be characterized. A time-resolved electrooptic (EO) sampling technique was used to measure the picosecond-order short transient, with a lithium tantalate ($LiTaO_3$) electrooptic crystal placed on top of the transmission line [9].

An output waveform from a photoconductive switch made from LT-GaAs on a vicinal (100) Si substrate and measured using EO sampling is shown in Fig. 4. The amplitude and width of the signal depend on sample growth conditions, anneal conditions, switch pattern, and testing parameters (e.g., optical pulse energy and bias voltage). There is always a tradeoff between the switch responsivity and speed. Dependence of the response on applied bias, optical pulse energy, and switch pattern was similar to that seen for devices made from LT-GaAs grown on GaAs substrates [4]. The main purpose of this study is to demonstrate the possibility of directly growing LT-GaAs on Si at low temperatures as an alternative to flip-chip bonding MSM switches made from LT-GaAs on GaAs material onto Si chips. We thus compare our LT-GaAs on Si with our earlier LT-GaAs on GaAs results [4] because the devices are identical and provide a direct comparison of the materials. The FWHM of the signal varies around 2 ps for both samples and the reference LT-GaAs on the GaAs sample. Fig. 5 shows a comparison of the photocurrent as a function of optical pump power for switches made from a LT-GaAs film on a vicinal Si substrate and the reference homoepitaxy wafer. It shows that the responsivity of the switch slowly saturates with increasing pulse power. This is expected since the carrier lifetime is very short. A large portion of carriers are trapped and recombine before they are collected by the electrodes. Therefore, the output photocurrent is mostly a manifestation of the number of captured photocarriers that are close to the MSM electrodes. At the constant pulse wavelength that we used at $\sim$850 nm, the number of carriers generated near the device surface and close to the electrodes will eventually

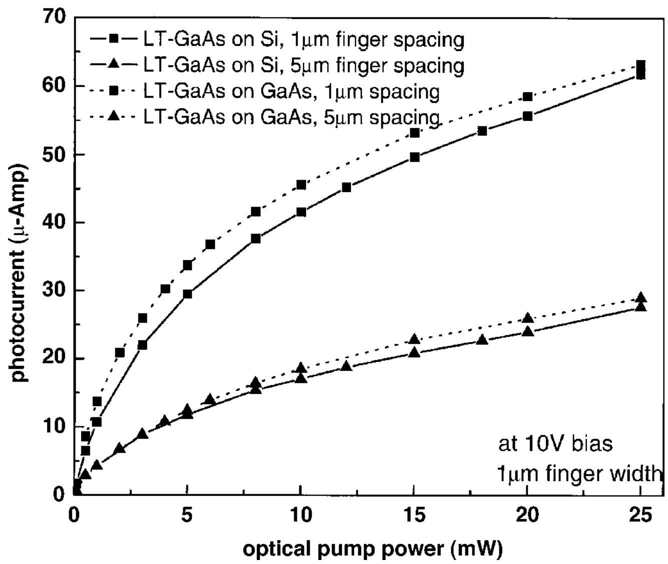

Fig. 5. Comparison of the photocurrent as a function of optical pump power for switches made from LT-GaAs films on vicinal (100) Si substrates and the reference LT-GaAs on GaAs wafer. The reference wafer is used in a demonstrated prototype two-channel ADC. Both types of switches have 1-μm finger width and the data shown were taken at 10 V bias voltage.

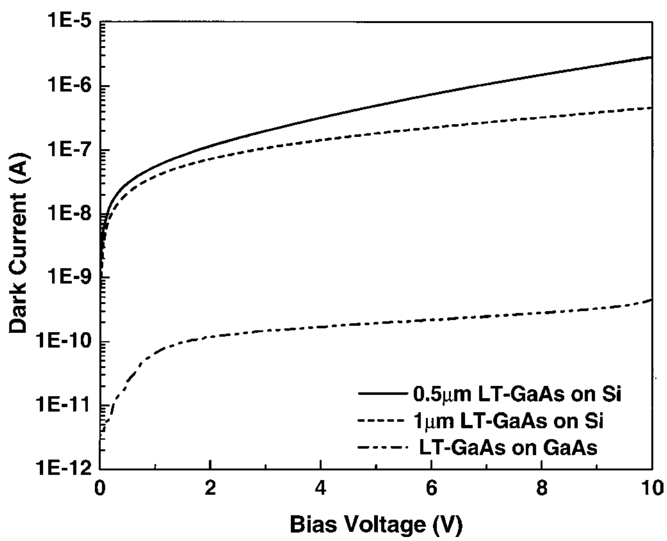

Fig. 6. Dark current of switches made from different materials. The two LT-GaAs on Si materials with different thickness were grown on vicinal (100) substrates under the same conditions. The LT-GaAs on GaAs wafer is the reference wafer used in a prototype ADC.

saturate as the optical pulse energy increases. In addition, the field-screening effect [10], [11] caused by excited photocarriers is more pronounced at higher optical pulse energy, which also contributes to the saturation behavior. The remarkable feature of this plot is that the responsivity of switches is quite comparable for LT-GaAs on Si versus LT-GaAs on GaAs reference wafer, although a high density of dislocations presumably exist in the material grown on Si substrate. Both switches have a 1-μm finger width. Fig. 5 also indicates that the responsivity increases with decreasing finger spacing, at the cost that device capacitance also increases for smaller finger spacing. Therefore, there is another tradeoff in choosing appropriate device size. The dark current is a primary concern for device applications. Fig. 6 shows that the dark current of LT-GaAs on Si switch is reasonably low, in sub—μ-Amp level, although it is approximately three orders of magnitude higher than the reference LT-GaAs on GaAs wafer. The switch made on a thicker (1 μm) LT-GaAs film exhibits lower dark current by moving farther from the defective Si-GaAs interface. To further reduce the dark current, we can incorporate an AlGaAs barrier layer between the GaAs and contact metal, or choose another contact material, such as WSi_x [12]. These features will be included in our future research. By optimizing the material quality and switch pattern, LT-GaAs grown directly on Si presents a promising alternative to bonding LT-GaAs on GaAs material to Si circuits.

III. Summary

We have grown GaAs directly on Si substrates at low temperatures (~250 °C). The wafer cleaning and film growth temperatures are safe for finished CMOS circuits. *In situ* RHEED patterns showed a clean, reconstructed Si surface before growth, and a reconstructed GaAs film after postgrowth annealing. AFM measurements reveal less than 1 nm rms roughness. XRD measurements indicate good film quality and negligible APD density. Time-resolved EO sampling characterization shows that the performance of LT-GaAs switches on an Si substrate is comparable to its homoepitaxy counterpart which was used in our prototype ADC which demonstrated outstanding performance. The successful low-temperature growth of GaAs on Si substrates promises the possibility of monolithic integration of ultrafast LT-GaAs switches with Si CMOS circuits, and further research is on the way.

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