4.6 Opportunities for Optics in Integrated Circuits Applications

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Optics brings opportunities for addressing two key problems in electronic chips and systems – interconnects and timing. Optics in principle enables dense, high-speed, long lines and solves problems of signal integrity (e.g., crosstalk, reflections, and voltage isolation) [1]; opportunities for off-chip interconnects are growing, and on-chip possibilities pose key questions [2]. Optical backplanes are under commercial development, and research shows promise for dense off-chip interconnects with hybridized lasers and modulators. Optics also allows radical concepts such as short pulse interconnects [3], with timing, sensitivity and latency enhancements, and wavelength division multiplexing [4], with higher line densities and ultimate compatibility with optical networks. All of these radical concepts have now seen laboratory demonstrations [3,4].

Short pulse optics offers many opportunities for precise timing, at least to key points on a chip [5]. Previous experiments have shown optical clocking of CMOS logic, with < 6ps output jitter, and optically triggered ADC's with < 80fs timing uncertainty [6]. Use of silicon CMOS photodetectors with blue light allows them to be efficient and fast [7], and could allow optical clock injection, for example, without receiver amplifiers or III-V devices.

One clocking application is for multiple clock phases in multiplexing data to high serial rates [8], with the maximum multiplexing determined by the clock timing accuracy. Lasers can provide stable sequences of short (e.g., 0.1-1ps) pulses, and the relative phase of each distributed clock can be set independently and precisely using optical path delays.

A 0.25μm CMOS test chip (Fig. 4.6.1) is implemented to show the potential benefits of using optical injection for multiple phase clocks in serial links. The chip includes clock phase multiplexers for measuring jitter and phase spacing/resolution of the optically injected clocks.

In an optical experiment, four clock phases, nominally spaced at 200ps, are brought onto photodiodes that directly drive chip circuits. Such diodes could be integrated on chip, though here commercial GaAs PIN wirebonded detectors are driven with the 850nm light short pulse light. Si detectors are included on the chip for future experiments. The optics shown in Fig. 4.6.2 generates four pairs of light beams using a beam splitter and two corner cube reflectors. The relative timing of the clock pulses is set by the position of the reflectors, noting that 300μm distance in free space gives 1ps of optical delay.

Each clock phase uses two photodiodes (Fig. 4.6.3). As each diode in the pair is alternately hit with a short optical pulse, the center point between the diodes is pulled first "up" then "down", giving a "rail-to-rail" voltage to a CMOS inverter input. The four clocks are then individually selected through a MUX (Fig. 4.6.4) to drive the output stage and to electrically measure jitter and phase spacing over a common electrical channel.

This optical clocking produced an output clock with 0.93ps rms jitter (Fig. 4.6.5). Figure 4.6.6 shows two adjacent phases tuned to ~200ps. Electrical clocks generated from a supply-regulated 5-stage ring-oscillator PLL [10] in the same 0.25μm technology, driven by an off-chip pulse generator, have 1.74ps rms jitter, and peak-to-peak phase variation of 11.3ps between the 5 electrical clock phases. In the ring oscillator, it is difficult to set this skew between the clock phases more precisely; in the optical case, adjacent phases can be set precisely by adjusting delay, though such precision is limited to two adjacent clock phases in the present optical setup. The 1.74ps electrical jitter may result from very careful design on a very quiet chip, and relies on direct electrical injection to the PLL from the precise external oscillator. The optical system is currently far from optimum, especially with the use of off-chip detectors.

These first experiments of picosecond optical clock injection show proof of principle that such injection is possible, with precise control over clock phase. In future work, on-chip silicon CMOS detectors will be investigated. Such detectors would eliminate inductive slew limits from bond wires (~10s of ps), and, with small detector element spacings, should allow much faster detector output slew rates, presumably further reducing clock timing uncertainty. Issues of optical power and alignment sensitivity and process variations in photodetectors remain open. The use of short pulse lasers may allow clocks with excellent frequency stability and phase control, at least to a small number of points on a CMOS chip.

References:

[1] D.A.B. Miller, "Physical Reasons for Optical Interconnection," *Int. J. Optoelectronics*, vol. 11, pp. 155-168, 1997.

[2] D.A.B. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," *Proc. IEEE*, vol 88, pp. 728-749, 2000.

[3] G.A. Keeler et al., "The Benefits of Ultrashort Optical Pulses in Optically-Interconnected Systems," *IEEE J. Sel. Top. Quantum Electron*. vol. 9, pp. 477-485, 2003.

[4] B.E. Nelson et al., "Wavelength Division Multiplexed Optical Interconnect Using Short Pulses," *IEEE J. Sel. Top. Quantum Electron*., vol. 9, pp. 486-491, 2003.

[5] C. Debaes et al., "Receiver-less Optical Clock Injection for Clock Distribution Networks," *IEEE J. Sel. Top. Quantum Electron.*, vol. 9, pp. 400-409, 2003.

[6] R. Urata et al., "Photonic A/D Conversion Using Low-Temperature-Grown GaAs MSM Switches Integrated With Si-CMOS," *J. Lightwave Technology*, vol. 21, pp. 3104-3115, 2003.

[7] A. Bhatnagar et al., "Pump-Probe Measurements of CMOS Detector Rise Time in the Blue," *J. Lightwave Technology*, vol. 22, pp. 2213-2217, Sept., 2004.

[8] C.-K. Yang, M. Horowitz, "A 0.8-μm CMOS 2.5 Gb/s Oversampling Receiver and Transmitter for Serial Links," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2015-2023, Dec., 1996.

[9] K.-Y. K. Chang et al., "A 0.4-4-Gb/s CMOS Quad Transceiver Cell Using On-Chip Regulated Dual-Loop PLLs," *IEEE J. Solid-State Circuits*, vol. 38, pp. 747-754, May, 2003.

[10] A. Emami-Neyestanak et al., "CMOS Transceiver with Baud Rate Clock Recovery for Optical Interconnects," *Symp. VLSI Circuits*, pp. 410-413, June, 2004.

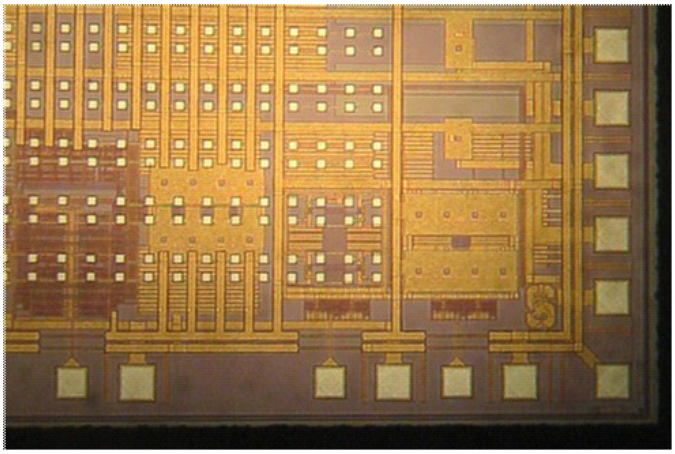

Figure 4.6.1: Optical clock-injection chip micrograph.

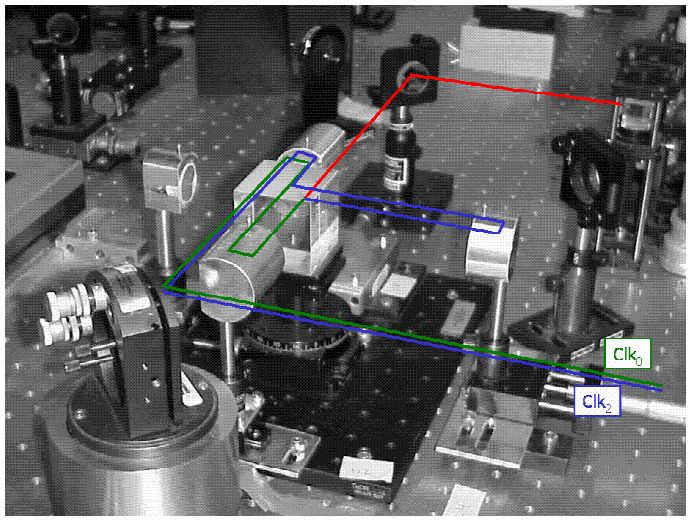

Figure 4.6.2: Optical setup for 4-phase clock spacing and distribution in which for simplicity two beams are shown.

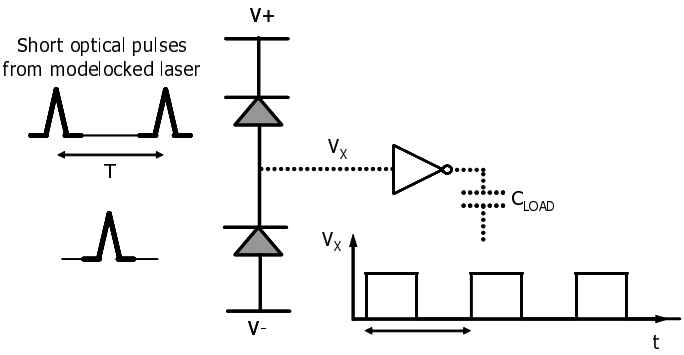

Figure 4.6.3: Generation of electrical clock using reverse biased photodiodes and short optical pulses.

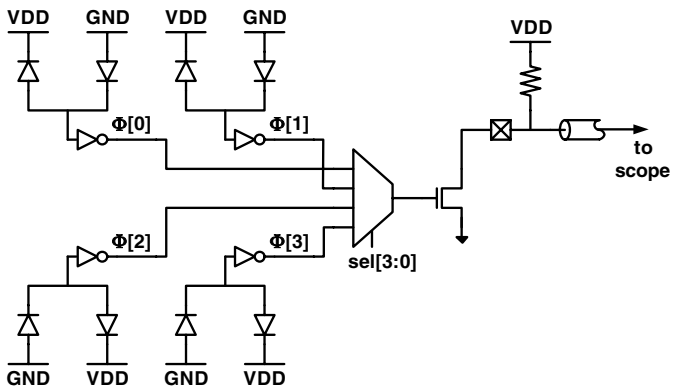

Figure 4.6.4: Optically Injected Clock MUX. The pairs of reverse-biased photodiodes shown are hit by alternating short optical pulses to generate clock signals.

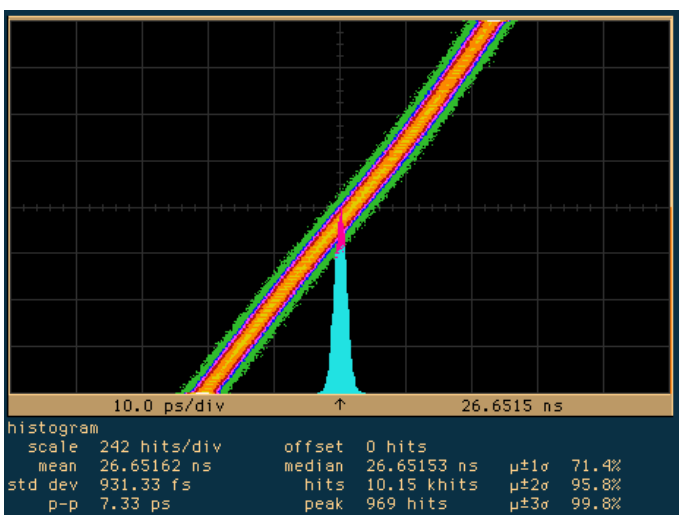

Figure 4.6.5: Jitter histogram for optically-triggered electrical clock output - GaAs PIN detectors driven with 850nm light.

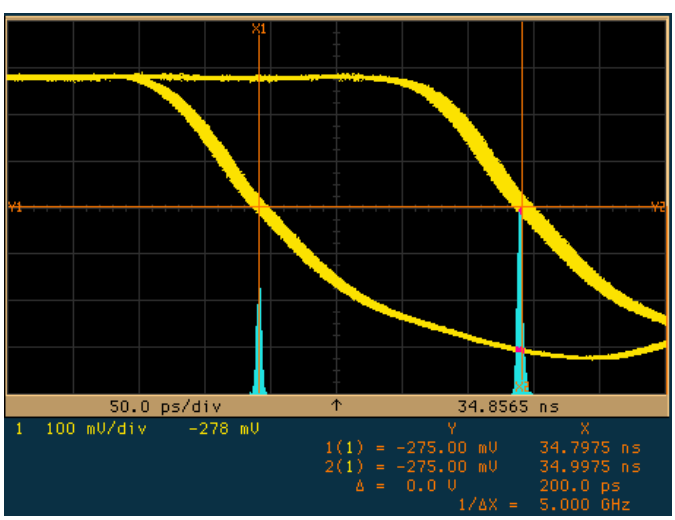

Figure 4.6.6: Phase spacing for optically-triggered electrical clock output.