Optimization of Absorption in Symmetric Self-Electrooptic Effect Devices: A Systems Perspective

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Abstract—**In this paper, the system switching speed or bit rate and signal beam tolerances of optical processing systems comprised of cascaded symmetric self-electrooptic effect devices (S-SEED's) are calculated as a function of the absorption characteristics of the devices. We show that the optimum design is neither simply one of best transmission contrast ratio nor of largest absolute difference between the "low" and "high" absorption states. Because the same diodes are used as detectors and modulators simultaneously, the optimum design for an S-SEED for best system performance is a compromise. We find that devices made by maximizing the ratio of the absorption coefficients in the "high" and "low" states while minimizing the change in applied electric field will give nearly "optimum" system performance.**

Introduction

QUANTUM-WELL electroabsorption devices have been proposed for use in optically interconnecting electronic circuits and for optical logic. Although there has been much progress in building these devices in recent years, only a limited amount of work has been done in trying to optimize the design of the devices for the best overall performance of the systems in which they would be used. In this paper, the relationships between the switching speed and signal beam tolerances of these systems are calculated as a function of the absorption characteristics of symmetric self-electrooptic effect devices (S-SEED's) [1]. This analysis will allow the design of more optimum devices. Additionally, the techniques described here can be applied easily to systems made using other optoelectronic devices.

The S-SEED is an attractive device to use in prototype optical signal processing systems. The device can act as an optical set-reset latch or as a differential logic gate capable of NOR, OR, NAND, and AND functions. In either case, the device has time sequential gain, provides for signal timing regeneration, is insensitive to optical power supply fluctuations and provides effective input-output isolation. In addition, because the signal inputs and outputs are differential in nature, absolute power levels are not critical, and operation of the device is possible over a power range spanning several decades. Like all SEED's [2], [3], the S-SEED relies on the changes in optical absorption that accompany a change in electric field applied perpendicular to the thin semiconductor quantum well layers. This effect is known as the quantum-confined Stark effect (QCSE) [4]. The QCSE has been demonstrated in several material systems, among them GaAs-AlGaAs, InGaAs-InP [5], InGaAsP-InP [6], and GaSb-GaAs [7], although to date the best SEED's have been made using GaAs-AlGaAs materials. Improved system performance might be achieved by making S-SEED's using other quantum-well structures, for example, coupled quantum wells [8], or asymmetric wells [9], [10]. Given the absorption characteristics of the devices, we will show how to calculate the extent of this improvement, and hence help choose the best quantum-well design.

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System Bit Rate

Systems based on these devices are made up of at least two stages of cascaded S-SEED flip flops or S-SEED logic gates. The devices are operated in a time sequential manner. First, low power signal beams set the state of the devices, and subsequently higher power clock beams read the state of the devices. After passing through the interconnection optics, the transmitted clock beams from one stage of devices become the signal beams for the next stage of devices. We consider two stages of devices; the clock beams read the state of the first stage of devices and set the state of the second stage of devices. The bit rate in a system is limited by the time it takes the photocurrent of the second stage of devices to charge the capacitance of the devices. This photocurrent is directly proportional to the optical power incident on these second stage devices. Therefore, the system bit rate can be found by first determining the absolute powers from the output of the first stage of devices that are incident on the second stage devices, and then calculating the switching time of the second stage devices from these inputs.

There are several methods of doing logic using S-SEED's. Among them are differential logic with preset beams [1], differential logic with output attenuators, dif-

ferential logic using both preset beams and attenuators [11], differential tristate logic [12], single ended and differential logic using electrically connected quantum-well diodes [13] (an extension of S-SEED's analogous to NMOS and CMOS circuits), and differential logic using sense amplification [14]. In this paper, we will calculate the system bit rate for cascaded S-SEED flip flops as illustrated in Fig. 1(a) and for differential logic with preset beams only, as illustrated in Fig. 1(b) for the preset beam applied to the bottom diode. The device can perform logic, even though its basic function is that of a set–reset latch, by ensuring that the device is in a given state using the preset beam. However, the general method of calculating system bit rate is the same for the other methods of performing logic as well.

The input and output logic levels are represented by the ratio of the optical powers in the two optical input or output beams. For example, we can define a logic "one" as when the power in the output beam coming from the top diode is greater than that from the bottom diode. For logic operation, the preset pulse generally has a larger amplitude than the signal beams because it does not have to propagate through a previous stage of the system. Therefore, the time that it takes to preset the device will be ignored. For the configuration in Fig. 1(b), the preset beam sets the SEED logic gate to a logic "1" with the upper diode more transmitting. After presetting, a second stage device will remain in its current state unless both outputs of the first stage devices are logic "ones" as defined above. Therefore, the logic gate in Fig. 1(b) is a NAND gate. The operation of a NOR gate is essentially identical, except that the preset beam is incident on the top diode and the device is thus preset in the state with the lower diode more transmitting. For S-SEED logic gates there are two sets of inputs that are both working to change the state of the device, but for S-SEED flip flops there is only one.

As we stated above, the first step in determining the system bit rate is to calculate the incident powers on the second stage devices. These powers are related to the incident clock power, the optical transmission (or reflectivity for a reflection mode device [15]), and the fan out of the first stage of S-SEED's and the optical losses between the two stages of devices. These powers, P_{in1} and P_{in2}, are given by

$$P_{in1}(t) = T[V_1(t)]P_{clk}(t)T_{opt}\,\mathrm{Fan}_{in}/\mathrm{Fan}_{out} \quad (1)$$

and

$$P_{in2}(t) = T[V_0 - V_1(t)]P_{clk}(t)T_{opt}\,\mathrm{Fan}_{in}/\mathrm{Fan}_{out} \quad (2)$$

where $T[V_1(t)]$ and $T[V_0 - V_1(t)]$ are the optical transmissions (reflections) from the quantum-well diodes in first stage devices at the relevant voltages, $P_{clk}(t)$ is the power in each clock beam, Fan_{in} is the fan in of the second stage of devices (either 1 for flip flops or 2 for logic gates), Fan_{out} is the fan out of the first stage of devices, and T_{opt} is the transmission of the optics interconnecting

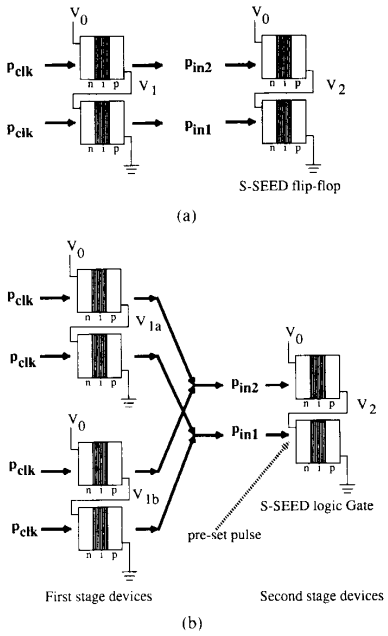

Fig. 1. Cascaded devices used in optical processing systems. (a) Cascaded S-SEED *S–R* flip flops and (b) cascaded S-SEED differential logic gates.

the devices. To calculate $P_{in1}(t)$ and $P_{in2}(t)$ using the above equations, we must first apply Kirchoff's current law to solve for the voltage $V_1(t)$ at the center node of the device assuming equal inputs, $P_{clk}(t)$ on each diode. We treat the currents as being equal to the incident power times a responsivity. This is essentially correct for reverse bias, and is a simple approximation for forward bias, although not strictly correct because the diode forward current is additive [3]. Therefore,

$$C_{tot}\frac{dV_1(t)}{dt} = S[V_0 - V_1(t)]P_{clk}(t) - S[V_1(t)]P_{clk}(t) \quad (3)$$

where $S[V_1(t)]$ and $S[V_0 - V_1(t)]$ are the responsivities (in A/W) of the two diodes in a first stage device and C_{tot} is the total capacitance of the two diodes. The problem of calculating the switching speed becomes much simpler if we assume that the first stage devices are completely switched before the clock beams are applied, removing the time dependence from (3). Then, the left-hand side of (3) can be set to zero. The resultant equation [(4)] can be solved for V_1.

$$S(V_0 - V_1) = S(V_1) \quad (4)$$

Since the S-SEED is bistable with equal input powers, there are three values for V_1 that satisfy (4), one ~ 0 V, one $\sim V_0$ V and one at $V_0/2$ V. The last value is unstable, and the other two correspond to the logic "zero" and logic "one" states of the device. Later, some simplifying assumptions about $S(V_1)$ will be made that allow us to set V_1 to 0 or V_0.

As stated above, once V_1 is known, the powers incident on the second stage devices are easily calculated from (1) and (2). The switching time can then be calculated by using Kirchoff's current law to solve for, in this case, the voltage $V_2(t)$, on the center node of the second stage S-SEED's as a function of time.

$$C_{\text{tot}} \frac{dV_2(t)}{dt} = S[V_0 - V_2(t)]P_{\text{in2}}(t) - S[V_2(t)]P_{\text{in1}}(t) \quad (5)$$

where $P_{\text{in1}}(t)$ and $P_{\text{in2}}(t)$ are the incident input power levels given by (1) and (2), $S[V_2(t)]$ and $S[V_0 - V_2(t)]$ are the responsivities of the two quantum-well diodes in A/W, and C_{tot} is now the total capacitance of a second stage device that needs to be charged with the photocurrent.

Equation (5) is of the form $C_{\text{tot}}[dV_2(t)/dt] = i[V_2(t)]$, where $i[V_2(t)]$ is the difference in photocurrents of the two diodes in a second stage device. One way to calculate the approximate switching time, is to divide the voltage change in going from one state to the other state into a number of small steps in voltage, δV_2 for which the current is approximately constant. Formally, we are simply integrating the differential equation (5). We can then calculate the switching time δt in each interval to be

$$\delta t = \frac{C_{\text{tot}}\delta V_2}{i(V_2)}. \quad (6)$$

Then, we can sum all of these interval switching times to get the overall time Δt.

$$\Delta t = \sum_{V_2 = \text{state1}}^{V_2 = \text{state2}} \delta t = \sum_{V_2 = \text{state1}}^{V_2 = \text{state2}} \delta V_2 \frac{C_{\text{tot}}}{i(V_2)}. \quad (7)$$

Since this still requires a detailed knowledge of the voltage dependence of the responsivity and transmission of the devices, we will simplify the absorption versus voltage characteristics to be constant at one level from zero to $V_0/2$ and constant at another level from $V_0/2$ to V_0. Therefore, the optical transmission is constant at one level T_{off} from zero to $V_0/2$ and constant at another level T_{on} from $V_0/2$ to V_0 as shown in Fig. 2(b). The subscripts "off" and "on" refer to either the voltage or the relative optical transmission of a particular diode (with "on" > "off"), and do not refer to the logic state of a S-SEED. We will also assume that the quantum efficiency is one for all voltages greater than zero (one electron for each absorbed photon), and zero for all voltages less than zero. Since the responsivity is proportional to the total absorbed light times the quantum efficiency, the responsivity is zero for all voltages less than zero, CA_{off} from zero to $V_0/2$, and CA_{on} from $V_0/2$ to V_0 as shown in Fig. 2(a), where A_{off} and A_{on} are the total light absorbed as a percentage of the input light in each of the two states, and C is a proportionality constant. It has been shown [2] that A_{off} must be greater than A_{on} for bistability to exist; this bistability is necessary in S-SEED's for time-sequential gain [1]. Operating the device at the wavelength λ_0 that maximizes the absorption (and responsivity) at 0 V bias ensures this.

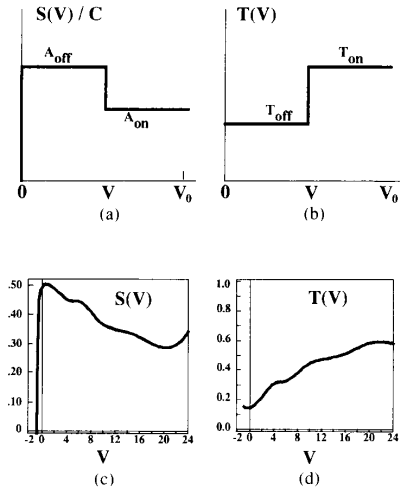

Fig. 2. Responsivity and optical transmission as a function of voltage of a single quantum-well p–i–n diode used at λ_0 in the S-SEED. (a) and (b) are responsivity and optical transmission using two-level absorption model. (c) and (d) are measured responsivity and optical transmission.

Actual measured characteristics for responsivity and optical transmission at this wavelength are shown in Fig. 2(c) and (d) for comparison.

From (7), recall that the system switching time in each interval depends inversely on the difference in photocurrents of the two diodes. This is illustrated graphically in Fig. 3(a). For logic operations, the second stage of S-SEED's are preset to a state where $V_2 = 0$ [see Fig. 1(b)]. From the two level absorption approximation, at $V_2 = 0$ the bottom diode of the second stage of S-SEED's has high absorption (high responsivity) initially and the top diode has low absorption (low responsivity). The first stage of S-SEED's are initially assumed to be in a state corresponding to the top diode having high transmission T_{on} and the bottom diode having low transmission T_{off} (i.e., $V_1 = 0$ or a logic "one" as defined earlier); otherwise the outputs from the first stage of devices will not switch the second stage. The initial photocurrents are shown in Fig. 3(a) at $V_2 = 0$. The current on the top diode (dark trace) is proportional to the input power $P_{\text{clk}}T_{\text{on}}$ times the absorbed light A_{on}. The current on the bottom diode (light trace) is proportional to the input power $P_{\text{clk}}T_{\text{off}}$ times the absorbed light A_{off}. During switching, the voltage V_2 gradually increases toward V_0. After V_2 has reached $V_0/2$, the absorption and photocurrents change. (In reality there is a smooth transition because the absorption is varying continuously as a function of voltage.) Now, the current on the top diode (dark trace) is proportional to the input power $P_{\text{clk}}T_{\text{on}}$ times the new absorbed light A_{off} and the current on the bottom diode (light trace) is proportional to the input power $P_{\text{clk}}T_{\text{off}}$ times the new absorbed light A_{on}. The difference in photocurrents in each of two time intervals can be seen from Fig. 3(a) to be proportional to $P_{\text{clk}}(T_{\text{on}}A_{\text{on}} - T_{\text{off}}A_{\text{off}})$ and $P_{\text{clk}}(T_{\text{on}}A_{\text{off}} - T_{\text{off}}A_{\text{on}})$. Thus, there are only two terms in the summation

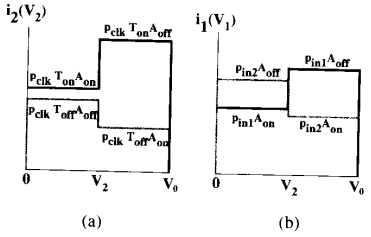

Fig. 3. Load line representation of a second stage S-SEED with light curve corresponding to the photocurrent of the bottom diode and dark curve corresponding to the photocurrent generated by the "load" diode for the cases where the device is (a) switching from the "low" state ($V_2 = 0$) to the high state and (b) where the device is being read out with (almost) equal clock beams.

in (7), and the switching time is equal to

$$\Delta t = \frac{kC_{tot}V_0/2}{P_{clk}}\left[\frac{1}{T_{on}A_{on} - T_{off}A_{off}} + \frac{1}{T_{on}A_{off} - T_{off}A_{on}}\right] \tag{8}$$

where $k = (h\nu\ \mathrm{Fan}_{out})/qT_{opt}\ \mathrm{Fan}_{in})$, $h\nu$ is the photon energy, and q is the charge of an electron. From Fig. 3(a), we see that the difference in the two photocurrents is smallest at the beginning of the switching period, and so the first term accounts for most of the switching time.

While, it is possible to make a S-SEED with separate diodes for detecting the signal beams and for modulating the clock beams, generally the same devices are used as modulators and detectors. Therefore the percentage of absorbed light and transmission of the devices are related by

$$A_i = 1 - T_i. \tag{9}$$

In this case, the switching time becomes

$$\Delta t = \frac{kC_{tot}V_0/2}{P_{clk}}\left[\frac{1}{T_{on}(1 - T_{on}) - T_{off}(1 - T_{off})} + \frac{1}{T_{on}(1 - T_{off}) - T_{off}(1 - T_{on})}\right]. \tag{10}$$

The bit rate of a system is equal to $1/2\Delta t$ since one bit period contains time to set the state and an equal amount of time to read the state of the device. The system bit rate is equal to

$$\text{bit rate} = \frac{1}{2\Delta t} = \frac{P_{clk}}{kC_{tot}V_0}\left[\frac{1}{T_{on}(1 - T_{on}) - T_{off}(1 - T_{off})} + \frac{1}{T_{on}(1 - T_{off}) - T_{off}(1 - T_{on})}\right]^{-1}. \tag{11}$$

We will define the *relative bit rate* as the bit rate is defined in (11) when $P_{clk}/kC_{tot}V_0 = 2\ \mathrm{s}^{-1}$. A value of 1.0 would indicate that the optical transmission of the first stage devices are 100 and 0% for the high and low states, respectively, and 100% of the light incident on the second stage devices is absorbed, regardless of which state the second stage devices are in. In practice, this can only be achieved by using separate detectors for the signal beams and modulators for the clock beams for the second stage S-SEED's since the detectors would have to absorb all of the light incident on them regardless of voltage. Using the *relative bit rate* to compare competing device designs assumes that the devices have the same size, voltage, quantum efficiencies, and wavelength of operation, since for the relative bit rate calculations we set $P_{clk}/kC_{tot}V_0$ or $P_{clk}(qT_{opt}\mathrm{Fan}_{in})/C_{tot}h\nu\mathrm{Fan}_{out}V_0)$ equal to a constant. Later, we will show that if we divide the relative bit rate by the applied electric field, we can compare device designs with different applied voltages and with different quantum-well thicknesses.

Beam Tolerances

Beam tolerances are related in both the signal beams and the clock beams, to the width of the bistable loop. In the case of the signal beams, we must ensure that their contrast ratio is greater than the width of the loop. In the case of the clock beams, the bistable region must be sufficiently wide to read out the state of the device without a small difference in clock power causing the device to switch. In addition, optical logic using preset beams without output attenuators requires a relatively wide bistable region since the two sets of inputs "balance" each other under the condition that one is a logic "one" and the other a logic "zero". If we place a limited amount of optical attenuation in the path of one of each pair of input beams (e.g., attenuate all "set" inputs), the signal beam tolerances can be relaxed [11]. As described in [11], in this case the signal beam tolerance only depends on contrast ratio and is independent of the bistable loop, although the bistable loop width is still important for the clock beams. However, the use of attenuators slightly complicates the optical system and increases the switching time for the system for a given amount of laser power.

To find the bistability width, consider the steady state input/output characteristics of the device calculated from (5) by setting $dV/dt = 0$. This gives

$$S(V_0 - V_2)P_{in2} = S(V_2)P_{in1}. \tag{12}$$

We will make the same assumptions that the absorption of the quantum-well diodes has one of two states. Fig. 3(b) shows the load line representation of the currents from each diode in the S-SEED in terms of the optical input powers P_{in1} and P_{in2}. The power range for which the device is in the bistable region can be found by inspection from Fig. 3(b), by considering that there must be intersection points at both 0 and V_0 V for the device to be bistable. For there to be an intersection point at 0 V, $P_{in2}A_{off} > P_{in1}A_{on}$. For there to be an intersection point at V_0 V, $P_{in1}A_{off} > P_{in2}A_{on}$. Combining these two inequalities in one equation, gives

$$\frac{A_{on}}{A_{off}} < \frac{P_{in1}}{P_{in2}} < \frac{A_{off}}{A_{on}}. \tag{13}$$

Recalling that $A_i = 1 - T_i$, one can rewrite (11) to get the conditions for bistability in terms of T_{off} and T_{on}.

$$\frac{1 - T_{on}}{1 - T_{off}} < \frac{P_{in1}}{P_{in2}} < \frac{1 - T_{off}}{1 - T_{on}}. \quad (14)$$

The output contrast ratio is, of course, given by

$$\text{output contrast ratio} = \frac{T_{on}}{T_{off}}. \quad (15)$$

For the case where both sets of signal beams are working to change the state of the device, the contrast ratio of these outputs from the first stage of devices must be sufficiently greater than the edge of the bistable region in order to switch a second stage device into a unique state. We will call the edge of the bistable region, the required input contrast ratio, which is merely given by the right-hand side of 14 or

$$\text{required input contrast ratio} = \frac{1 - T_{off}}{1 - T_{on}}. \quad (16)$$

The signal margin can be defined as the ratio of the output contrast ratio, T_{on}/T_{off} to the required input contrast ratio, $(1 - T_{off})/(1 - T_{on})$. This ratio is given by

$$\text{signal margin} = \frac{T_{on}(1 - T_{on})}{T_{off}(1 - T_{off})}. \quad (17)$$

For cascaded flip flops, by maximizing the signal margin, we maximize the allowed variations between the set and reset signal beams. For cascaded logic gates, maximizing the signal margin maximizes the allowed variations of the signal beams in the case when both beams are working to change the state of the device. However, in the case where the two logic inputs are different, maximizing the required input contrast ratio maximizes the allowed variations in the signal beams. Therefore, for logic operations, both a wide bistable loop width and a high signal margin are important.

Experimental Results

To check the above simplifications for accuracy, the responsivity and transmission (or reflectivity of a reflection mode quantum well p–i–n diode [15]) must be measured as a function of voltage. If we ramp the voltage on a S-SEED from zero to a voltage V while the optical input powers on the two diodes are unequal, the diode with the largest incident power remains forward biased (~ 1 V), and the diode with the least incident power remains reverse biased with a voltage equal to $\sim(V + 1)$ [12]. The current equals the responsivity of the diode with the least incident power times this power. Subtracting ~ 1 V from the current–voltage and reflectivity–voltage measurements gives us the correct characteristics for a single diode. We measured these characteristics for reflection mode S-SEED's with 5×10 μm windows [16] using an argon-ion-pumped Ti:Sapphire laser at 849 nm at optical input power levels of the two inputs of 50 and 100 μW, respectively, [see Fig. 2(c) and (d)] and again at 500 μW and 1 mW, respectively. We also measured the bistable input/output characteristics by sinusoidally varying the power of one of the two inputs while holding the power constant on the other input. Bistable characteristics were measured at (constant) powers of 50 and 500 μW at supply voltages of 11 and 19 V. The results of both sets of measurements are shown in Table I. In all cases, the bistability width using the simplifications outlined in the previous section is larger than the actual measured bistability width. This is most likely due to recombination within the diodes at low voltages, most likely surface recombination on the mesa sidewalls [17], which reduces the internal quantum efficiency or percentage of absorbed photons that become photocurrent. Since this recombination has no effect on absorption, the photocurrent and responsivity are less than would be predicted from the absorption alone, and the bistability width is reduced from what it would be if there were no surface recombination.

As a simple system demonstration, a photonic ring counter has been built using two of these devices as illustrated in Fig. 4 [18]. The input clock powers (in the "clock on" state) to the S-SEED's were 484 and 550 μW for the two S-SEED's. The transmitted light from the output of S-SEED #1 to the input of S-SEED #2 was 31%. The transmitted light from S-SEED #2 to S-SEED #1 was greater, so the clock power incident on S-SEED #1 limits the speed of the system. We had difficulty making the system work at greater clock powers, because of saturation effects in the quantum well material [19]. Saturation degrades both the contrast ratio and bistability width. In fact, because of this saturation of the quantum-well material, they are already degraded severely at 500 μW compared to 50 μW. The measured switching time of the ring counter was ~ 40 ns. Using (9), with $C_{tot} = 23$ fF $= h\nu/q = 1.46$, $V_0 = 11$ V, with fan in and fan out of 1, gives a switching time of 32 ns. The difference between the calculated and measured switching times is most likely due to extra charge required to switch the device, perhaps from excess parasitic capacitances, because the measured optical switching energies of these devices are also higher than expected from simple calculations. However, the prediction is close enough that the performance of one type of device relative to another may be compared with reasonable confidence. It is interesting to note that the degradation in contrast ratio because of saturation causes the bit rate at 500 μW to be a factor of two worse than at 50 μW, when normalized by the input power. Future improved quantum well designs are expected to alleviate this problem [20].

Discussion

The output contrast ratio [(15)], required input contrast ratio, [(16)], signal margin [(17)], and relative bit rate [(11) with $P_{clk}/kC_{tot}V_0 = 2\ s^{-1}$] are the four characteristics of the devices and systems that we will consider when comparing device designs with different characteristics. In Fig. 5(a)–(d) these four characteristics are plotted as a function of the two transmission states of the devices T_{off} and T_{on}. There is not one universal parameter that we can look at to get the best performance in a systems, but all four of these characteristics are important.

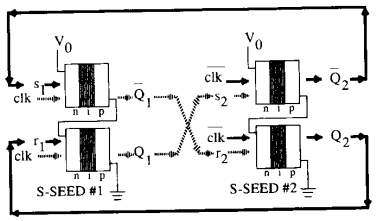

Fig. 4. Block diagram of photonic ring counter constructed by cascading two S-SEED's with the interconnections shown. The actual devices that were used in the experiment were reflection mode devices.

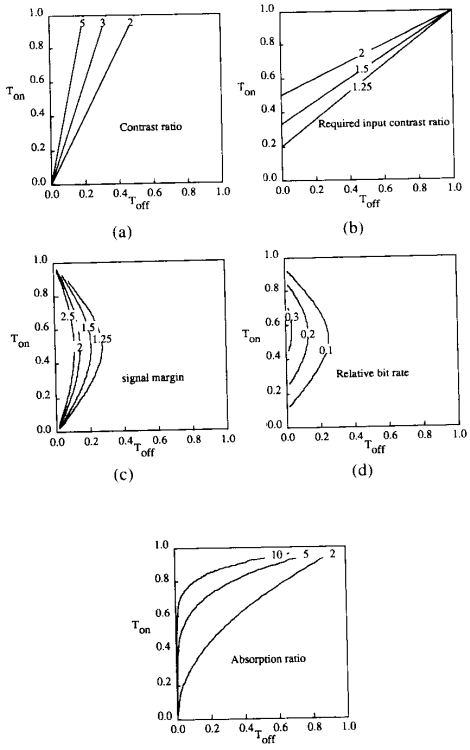

Fig. 5. Characteristics of S-SEED devices and systems as a function of the optical transmission of the devices in the highly transmitting and highly absorbing states. (a) output contrast ratio [T_{on}/T_{off}, see (15)], (b) required input contrast ratio [$(1 - T_{off})/(1 - T_{on})$, (16)], (c) signal margin (i.e., output contrast ratio divided by required input contrast ratio, (17), (d) relative bit rate [(11) with $P_{clk}/kC_{tot}V_0 = 2\ s^{-1}$]. A value of 1.0 corresponds to the p-i-n diodes in the first stage devices either transmitting or absorbing 100% of the incident optical clock power and the second stage devices absorbing 100% of the incident signal power, (e) is the ratio of absorption coefficients of the devices, α_{off}/α_{on} in the highly absorbing to highly transmitting state.

For example, it is obvious that we want to maximize the bit rate in a system, but we also must consider that the device should have a good signal margin (which we recall is equal to the ratio of the output to required input contrast ratios) and a wide bistable loop width so that the system will be tolerant to fluctuations in relative powers of the optical signals. It is fortunate that the best relative bit rate and best signal beam tolerances occur at nearly the same range of values for T_{off} and T_{on}.

From Fig. 5(a)–(d), several key points that should be made. The first is that the maximum output contrast ratio by itself is *not* a good thing to optimize. For example, if the two transmissive states are given by 10 and 0.1% (a 100:1 output contrast ratio), the relative bit rate of the system [calculated from (11) with $P_{clk}/kC_{tot}V_0 = 2\ s^{-1}$] is rather slow (0.084), because only a small fraction of the power from the clock beams on the first stage reaches the second stage. Additionally, the bistable loop is quite narrow when both states have high absorption [see (14)], meaning that the tolerance on the clock powers becomes severe.

Another misconception is to optimize the *difference* in the two transmission states of the device (i.e., $T_{on} - T_{off}$). For example, a device with transmission states of 60 and 10% would yield a higher system bit rate and allow greater beam tolerances than a device with 80 and 10%. This is because there is a balance between maximum absorbed power and maximum transmitted power that will give the optimum speed and tolerances of the devices in a system. If there is insufficient absorption in the high transmission state, there will be too little photocurrent generated when we try to change the state of the device by shining a strong beam on this diode, and thus the device takes longer to switch. The optimum relative bit rate is with transmission states of 58.6 and 0% giving a maximum relative bit rate of 0.34. With T_{on} varying from 54 to 63% and T_{off} equal to 0%, the relative bit rate is within 1% of this optimum. Although devices with very low reflectivities in the off state have recently been reported using resonant cavities [21], allowing 10% transmission in the low state, with 60% in the high state still gives a device with good performance. The relative bit rate would be 0.23, or 2/3 that of the optimum, the output contrast ratio would be 6, the required input contrast ratio would be 2.25 and the signal margin would be 2.67 (output divided by required input contrast ratios). Since such a device would have both a high signal margin and a wide bistable loop width, it will be tolerant to both variations in signal and clock powers.

The absorption coefficients required to get the desired optical transmissions can be calculated from $-\alpha_i L = \ln T_i$. Fig. 6(a)–(d) replot the output contrast ratio, required input contrast ratio, signal margin, and relative bit rate as a function of $\alpha_{off}L$ and $\alpha_{on}L$. In Figs. 6(e) and 5(e) contours of α_{off}/α_{on} are plotted as a function of $\alpha_{off}L$ and $\alpha_{on}L$ and T_{off} and T_{on} with the optical path length of the device changing as one moves along the curves. This ratio of α_{off}/α_{on} must be greater than ~ 5 to approach the optimum system bit rate. For the QCSE devices that have been made so far, operation at the exciton peak at zero field λ_0 will give an absorption coefficient ratio of only ~ 2 at an applied electric field of $\sim 5 \times 10^4$ V/cm. Therefore, changing the optical path length of the device (thickness of the well region) will only result in movement along a particular curve shown in Figs. 5(e) and 6(e).

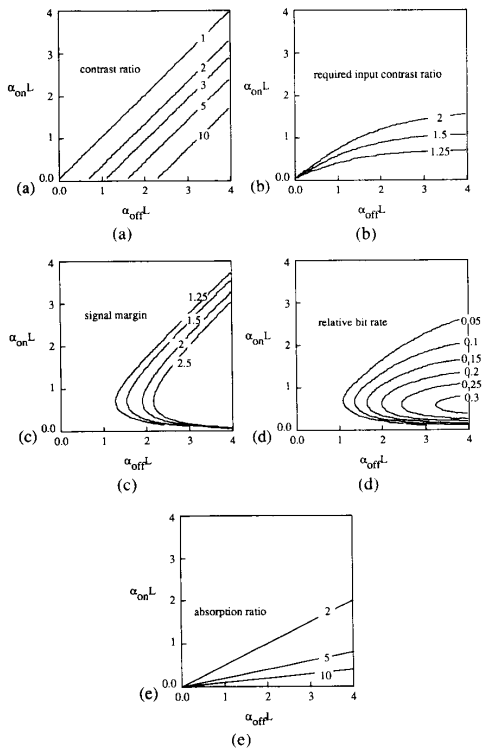

Fig. 6. Characteristics of S-SEED devices and systems as defined in Fig. 5 as a function of the optical absorption lengths of the devices in the highly transmitting and highly absorbing states. (a) output contrast ratio, (b) required input (a) output contrast ratio, (b) required input contrast ratio, (c) signal margin, (d) relative bit rate, and (e) α_{off}/α_{on}.

Although there is an optimum length, the best performance would be achieved only with a larger absorption coefficient ratio. Also, it is somewhat difficult to make thick quantum well regions, so the absorption coefficient in the low absorbing state should be at least 2500 cm^{-1} so that with two passes through 1 μm of quantum-well material will give an optical transmission of 60%. If there is not enough absorption in each of the two states, but the ratio of the two absorption coefficients, α_{off}/α_{on} is large enough, placing the quantum-well region within a resonant cavity [21] can increase the effective path length of the device.

We stated earlier that the relative bit rate can be used to compare different device designs of the same physical size operating at the same voltages. It is shown in [3] that the switching energy of the devices is proportional to the change in electric field that occurs across each diode when the device changes state. Therefore we would expect the system bit rate to depend inversely on the applied electric field; that is, a higher electric field means a slower bit rate. We will show this below. The change in electric field between the on and off states of the device ΔE is given by

$$\Delta E = V_0 L \tag{18}$$

where L is the thickness of the multiple quantum-well region of the device. The capacitance of the device is given by

$$C_{tot} = \epsilon A/L \tag{19}$$

where ϵ is the permittivity of the material and A is the total area of the device, assuming that we model the device as a parallel plate capacitor. Substituting these relationships into (11) gives the bit rate in terms of ΔE as

$$\text{bit rate} = \frac{P_{clk}}{k\Delta E \epsilon_r A}\left[\frac{1}{T_{on}(1-T_{on}) - T_{off}(1-T_{off})} + \frac{1}{T_{on}(1-T_{off}) - T_{off}(1-T_{on})}\right]^{-1} \tag{20}$$

where again $k = (h\nu \text{Fan}_{out})/(qT_{opt}\text{Fan}_{in})$. Because of the dependence of the bit rate on the electric field in the denominator of (20), dividing the relative bit rate calculated using (11) for $P_{clk}/kC_{tot}V_0$ equal 2 s^{-1} and plotted in Figs. 5(d) and 6(d) by the applied electric field gives a way to compare devices of different thicknesses operating at different electric fields.

When operating at λ_0, greater absorption coefficient rations and higher output transmission in the high state can be achieved at higher applied fields. The system bit rate may improve or may get worse at these higher fields depending on whether the improved characteristics offers more benefit than the detrimental effect of the higher electric field. As an example, consider the device measurement at 500 μW shown in Table I. At 11 V bias, the relative bit rate divided by the applied electric field is equal to 7.1×10^{-7} (0.078 divided by 11×10^4). At 19 V bias, the device has better characteristics and the relative bit rate for the system is 0.10. However, when we normalize the relative bit rate by the increased applied electric field (19×10^4), the result of 5.26×10^{-7} indicates that the actual bit rate with 19 V would be less than it was at 11 V. The optimum applied electric field that maximizes the system bit rate can be found by calculating this "normalized" relative bit rate at all applied electric fields, but as we stated earlier, signal margin and bistability width must also be considered. When considering new devices designs, the ratio of absorption coefficients in the two states should be maximized while the electric field required to achieve the absorption change should be minimized.

Because a balance exists between using a quantum-well diode as a detector and as a modulator, higher system bit rates may be obtained by making S-SEED's with separate detectors for the signal beams and modulators for the clock beams. In this case, for the maximum bit rate, we merely optimize the difference in the two modulator transmission states (again not the ratio). The best relative bit rate with all power absorbed in the detector and transmission states of 100 and 0% is 1.0 (the standard against which all other speeds in Figs. 5(d) and 6(d) are normalized). However, with fully absorbing detectors, there would be no bistability while the input signals are applied. For logic operations where the two inputs have different logic states,

TABLE I
CALCULATED AND MEASURED INPUT AND OUTPUT CONTRAST RATIOS FOR INPUT POWERS OF 50 AND 500 μW AT POWER SUPPLY VOLTAGES OF 11 AND 19 V. ALSO SHOWN IS THE RELATIVE BIT RATE IN A SYSTEM [FROM (11) WHEN $P_{clk}/kC_{tot}V_0 = 2\ S^{-1}$] AND THE CALCULATED AND MEASURED SPEEDS OF A PHOTONIC RING COUNTER CONSTRUCTED USING THESE DEVICES.

Incident "On State" Clock Power/Beam	50μW		500 μW	
dc voltage	11 V	19 V	11 V	19 V
S-SEED reflectivities-T_1	15%	15%	25%	25%
T_2	46%	58%	40%	54%
Calc. output contrast ratio	3.1	3.8	1.6	2.2
Calc. input contrast ratio	1.6	2.0	1.3	1.6
Measured output contrast ratio	2.8	3.5	1.6	2.0
Measured input contrast ratio	1.3	1.6	1.2	1.4
relative bit rate [Fig. 5(d)]	0.174	0.185	0.078	0.10
ring counter system switching time (calc.)	138 ns	224 ns	31 ns	41 ns
ring counter system switching time (meas.)			40 ns	

bistability *is* required during the application of the signal beams. Therefore, for a device with fully absorbing detectors, one of the other methods for doing logic could be used, for example logic with the selective attenuation of the input beams. For operation as cascaded flip flops, the device does not require bistability during the application of the input beams because with a single set of inputs, the device will still switch toward one of the two power supply rails. When the clock beams are applied, the device is bistable and thus read out in one of its two stable states.

In the arrays of S-SEED's that have been made so far [16], [23], the measured optical transmissions of the two states are ~46 and 15% at 11 V bias and 50 μW as shown in Table I. By using separate modulators and highly absorbing detectors the relative bit rate would be improved from 0.174 to 0.31. The reason for the relatively small improvement is that, even in the highly transmitting state, over half of the light is already absorbed. However, by making perfect detectors and modulators, the system bit rate (for cascaded flip flops) would be improved by a factor of more than five over the current devices.

CONCLUSION

In the conclusion, we have shown how to calculate the bit rate and relative beam tolerances (as related to the width of the bistable loop) of photonic switching and optical computing systems using S-SEED's. We have used a simple two level absorption versus voltage model to find the optimum values of optical transmission and absorption coefficients in the high and low states in terms of the output contrast ratio, required input contrast ratio, signal margin, and system bit rate. When using quantum well diodes as modulators and detectors simultaneously, the optimum transmission in the high state should be ~60% while keeping the transmission in the low state below 10%. This requires that the ratio of absorption coefficients in the two states be greater than ~5. To further improve system performance it is necessary to reduce the change in electric field required to achieve this ratio of the absorption coefficients. Finally, using separate detectors and modulators may be able to improve performance as well.

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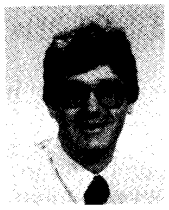

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