DENSE TWO-DIMENSIONAL INTEGRATION OF OPTOELECTRONICS AND ELECTRONICS FOR INTERCONNECTIONS

by

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Dense two-dimensional integration of optoelectronics and electronics for interconnections

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ABSTRACT

Optics has many features, beyond those already exploited in long-distance fiber communications, that make it interesting for interconnections at short distance, including dense optical interconnections directly to silicon integrated circuit chips. Hybrid technologies, such as solder-bump bonding, have recently been successfully used to attach two-dimensional arrays of optical detectors, emitters, and modulators to silicon electronics. Quantum well modulator or self-electro-optic-effect devices (SEEDs), and vertical-cavity surface-emitting lasers (VCSELs) have received particularly strong attention as candidates for the necessary arrayed output devices. This article summarizes the research and prospects in these fields.

1. INTRODUCTION

The problems with using conventional electrical wiring for sending signals over long distances are well known. One consequence has been the introduction of optical fiber for long-distance communications. Increasingly, optics is being used for shorter distances, such as fiber distribution networks for cable television, and for local networks, for example on a campus scale. Optics is now also being used at some shorter distances, such as for connection to peripherals in computer systems, and the first multiple-fiber products for interconnection between cabinets are now being introduced. The possibility of using optics for interconnection at even shorter distances is one that has been a subject of considerable research and analysis (for early work, see, for example Goodman et al.[1] and Feldman et al.[2]) At these shorter distances, there are many physical reasons beyond the problems of loss on electrical wires that make optics an attractive alternative.[3]

The additional potential features of optics for interconnection at short distances include (a) reduction of power and area consumed by interconnect drivers and pads on chip, (b) avoidance of frequency-dependent cross talk, (c) avoidance of problems from pin inductance on chip signal and power lines, (d) avoidance of wave reflection phenomena on boards and backplanes, (e) reduction of signal and clock skew within the system, (f) voltage isolation, (g) electrical noise immunity, (h) increased density of interconnections to chips, and (i) possibilities for highly-interconnected global topologies.

In addition, the use of optics can enable existing architectures to continue to scale to higher speeds and capacities because optics avoids problems associated with the so-called "aspect ratio" limit of electrical wiring, a limit that is particularly important for highly-interconnected architectures that might be encountered in, for example, switching or multiprocessor systems.[4] An additional reason for moving to optics for interconnection

has to do with ease of design and elimination of non-recurring engineering costs; an optical system designed for use at 100 MHz does not have to be redesigned as the speed of the system is increased since nothing about the propagation of the optical signals through the optics changes substantially for any conceivable modulation rate that the electronic system could generate (though, of course, faster devices would be required). This is in stark contrast to the situation with electrical back planes, for example, where the wiring needs substantial and careful redesign as the speed of the system is increased.

To take advantage of power and size reduction, increased interconnection density, or dense interconnection to chips or multi-chip modules, requires optoelectronic technology and integration that goes well beyond what has been used for telecommunications, data links, networks, and existing multiple-fiber interconnect technologies. Specifically, techniques for the dense integration of optoelectronics with mainstream electronics have to be devised that allow both high density and high performance in terms of speed and power dissipation. Fortunately, the very act of good integration can substantially improve the performance of the system, in particular, reducing the power dissipation of receiver circuits,[5] which otherwise could be a substantial limit on integration density.

One very interesting prediction[5] is that, as the silicon electronics technology advances for digital circuits, the performance of optoelectronic receiver circuits in the same technology would also increase so that optical interconnects to chips could keep pace with the advances in the ability of silicon chips to perform logic operations, a scaling that electrical interconnects do not show. In general, the fact that electrical interconnects do not scale well is becoming very well known and understood in the electrical community, and optics is perhaps the only viable physical technology that offers serious promise of circumventing this scaling limit.

Historically, the absence of low-power optoelectronic output devices capable of integration in large arrays prevented any serious dense integration to electronic chips or modules. Fortunately, however, the development of novel optoelectronic devices over the last decade has changed that situation. Now, it is not necessary to restrict systems to use the relatively high power consumptions and sizes associated with, for example, the lasers used for long-distance communications. The development of lasers with lower threshold currents, and the emergence of viable modulator technologies with no threshold behavior at all, has opened the way for serious dense integrations. Also, both the quantum well modulator or SEED and the VCSEL offer devices that can operate for light beams propagating perpendicular to the surface (so-called "surface-normal" operation), which allows both new possibilities for packaging one-dimensional arrays and the ability to make two-dimensional arrays. The quantum well modulators or SEEDs in particular have demonstrated impressive abilities to be successfully integrated with electronics in very large arrays.[6-14]

In this article, we will review the attempts to achieve large-scale integration of optoelectronic devices with mainstream electronics. The article will emphasize the use of solder bonding techniques for hybrid integration since these are, at the moment, the most highly developed methods for such large integrations. We will also discuss the various possible devices for such integrations, and summarize the progress to date. Space will not permit an exhaustive review of all of the literature in this broad subject area. Except for

subjects central to this review, references will unfortunately often have to be restricted to other reviews or to recent examples of work in the field.

2. RATIONALE FOR DENSE INTEGRATION WITH MAINSTREAM ELECTRONICS

It is obviously most desirable to be able to have an efficient and manufacturable integration of any desired optoelectronic devices to mainstream electronics. The ability to use mainstream electronics means that all of the existing electronic design and manufacturing tools can be exploited so that there is little or no constraint in the kinds of systems that can be made. Ideally, such an integration would impose no restrictions on the electronic technology itself. With the ability to use mainstream electronics, the resulting combined electronic and optoelectronic technology would be able to address the largest number of applications, and hence would be most likely to be introduced. There is clearly a great need for standardization of such integration round about a standard electronic platform so as to reduce the cost of introduction of the optoelectronics.

There have in the past been several quite successful attempts to make optoelectronic logic arrays based on logic technology other than standard electronics. Examples include the symmetric self-electro-optic-effect device (S-SEED) technology,[15,16] the double-heterostructure optoelectronic switch (DOES),[17] the V-STEP,[18] and photothyristors.[19] These devices proved explicitly that the conversion from optics to electronics and back to optics could be very efficient and fast, and take up relatively small areas. The power and area efficiency demonstrated in these devices contradicted a prevailing myth, derived primarily from experience with telecommunication systems, that the conversion between optics and electronics was necessarily a process that took much power and area and entailed substantial delay. These device technologies also showed that two-dimensional optoelectronic technology was quite feasible, and allowed both the testing of simple functioning digital optoelectronic information processing systems[10, 11, 20, 21] and the practical demonstration that it was quite feasible to work with large two-dimensional arrays of light beams in digital systems. These technologies also lead to the concept of "smart pixels,"[22] two-dimensional arrays of units with both optical inputs and optical outputs combined with varying degrees of smart functionality (either analog or digital) between the inputs and outputs.

The weakness of these technologies was not necessarily the difficulty of making arrays of functional devices (though some technologies were more successful than others in this), but rather that systems seemed to demand greater logical sophistication between input and output than was available from these technologies that relied on relatively simple custom optoelectronic logic. It also became clear from experiments with this class of two-dimensional optoelectronic device arrays that optical power was an important constraining commodity, and hence systems that could incorporate some gain so that optical input powers could be reduced would be highly desirable. Hence, the desire both to allow more sophisticated functionality and to reduce optical input powers whenever feasible led to the desire to integrate with conventional electronics if possible.

In integrating the optoelectronics and the electronics, it is also highly desirable that the integration can be dense — that is, with large numbers of optoelectronic devices per unit area. Dense integration allows the optoelectronics to attack any of the problems in

electrical systems that occur at high densities of interconnection. It would allow, for example, interconnect densities not only beyond those of current edge connectors on boards, but also even substantially beyond the current numbers of "pin-outs" available with even the highest density electrical chip connection technologies. Dense integration would also allow optics to be considered even for key "long-distance," high-speed interconnects within a given chip.

Integrating at high density requires devices that themselves have high yield and low power consumption, and, importantly, receiver and transmitter circuits for those devices that also have low power consumption. Such devices and circuits would give efficient optical-to-electrical conversions. Arguably, however, to achieve these efficiencies also requires integration. The lack of integration in current interconnects, data links, and long-distance telecommunication optoelectronics is one of the reasons why such systems are relatively large and consume a lot of power.

Integration allows the optoelectronic devices to be smaller themselves (for example, they do not need to be large enough to have pads for wire bonding), and this small size means the devices are likely to have small capacitance. In addition, the integration technology can also be one with very small parasitic capacitance. The resulting low total capacitance is very important for the design of the receiver circuits, since it can result in simpler circuits with low power dissipation and small area. In typical receiver circuits for long-distance telecommunications, for example, the capacitance of the input photodiode, because it is large and may be wire bonded to the receiver circuit, may be of the order of 1 picofarad. The optimum design of receiver circuits for low noise typically requires that the capacitance of the input field-effect transistor is comparable to that of the photodiode code.[23] The resulting field-effect transistor is therefore relatively large because the input stage in the amplifier must be biased with a steady drain-source current so that it can function as a small signal amplifier. Because the input field-effect transistor is large, the resulting current and power dissipation of such receiver circuits is also large. By efficiently integrating a small photodetector with low stray capacitance (e.g., ~50 fF), it is not necessary to run with such large field-effect transistors, and hence the power dissipation is reduced for the circuit, as also is the circuit's area.[5]

Incidentally, the optimum design of receiver for interconnect applications is likely not one that is receiver-noise limited. Though reasonably low operating powers are desirable for optical interconnects, there is likely no need to go to the extreme sensitivity of, for example, long-distance telecommunications receiver circuits. Input optical powers in interconnects might be in the range of 1-100 microwatts, allowing receivers with fewer gain stages, and allowing the input transistor to be physically smaller still with even less power dissipation. Smaller optical input powers could result in a receiver too susceptible to extraneous noise and with too high a power dissipation. Larger optical powers could result in too high a dissipation in the optical transmitter circuits and devices. One likely design of receivers for dense interconnects using conventional approaches would be a two- to three-stage receiver with transistors of dimensions close to the minimum size in a given technology.[5]

It would, of course, be possible to perform monolithic integrations of optoelectronics and electronics to achieve these goals of low parasitic capacitance and high performance. Indeed, it is actually likely that such monolithic integration would, in the end, give the

very highest performance. There have been successful attempts at monolithic integration, notably the FET-SEED process,[24] which was used to demonstrate complex circuits that were used in switching systems experiments,[21] and also successful integrations of detectors, field-effect transistors, and modulators[25] or VCSELs.[26] The difficulty with such systems is that the electronics technology used is not that of mainstream electronics. In particular, it is not silicon CMOS (an integration of detectors and LEDs with a commercial GaAs VLSI process was successfully demonstrated, however[27]). Hence the complexity of circuits that can be fabricated is limited, both by the physical yield of the non-standard electronic technology, and the lack of very highly developed design tools for the custom electronics technology being used.

It is not impossible to integrate III-V compound optoelectronic devices monolithically with silicon CMOS, i.e., in which the device is physically grown onto the silicon material. One problem is that, for most light emitters, there typically are problems with device lifetime, often attributed to the high defect density associated with the lattice mismatched growth of the III-V materials on silicon substrates. Propagation of "dark-line" defects is a common cause of failure in optoelectronic light-emitting devices. Examples of devices monolithically integrated with silicon included LEDs[28] and quantum well modulators.[29] The modulators have been demonstrated to have long lifetimes, perhaps because they are reverse-biased rather than forward-biased devices. Even if the lifetime problem is solved, however, there still is the issue that the fabrication process for the electronics has to be changed somewhat to accommodate the optoelectronic monolithic integration, and any such change would likely result in substantial cost. This therefore means that there would be a high economic barrier to the introduction of a monolithic integration with mainstream electronics.

Hence, there are very strong arguments for a hybrid integration technology that would allow integration of any desired optoelectronic device, in large numbers, with low capacitance and small device size, to existing and future generations of mainstream electronics without modification of the fabrication process for the mainstream electronics itself. Arguably, all of these criteria can be met by using hybrid techniques such as solder bonding to silicon CMOS.

3. BONDING TECHNOLOGY

Given that we want to attach large numbers of optoelectronic devices to silicon CMOS circuits, we need ideally to find technologies that already exist, or could be amended for, this purpose. One obvious place to start is to attempt to exploit technologies already developed for the packaging of electronic chips. Though to this day most packaging of chips involves wire bonding, since the 1960s other techniques have been used, especially so-called "flip-chip" technology. Such techniques allow large numbers and high densities of connections to the surface of a chip by bonding it face-to-face with some other substrate with appropriate electrical connections. In the case of using such techniques for optoelectronic device attachment, the same basic philosophy can be used to attach the optoelectronic devices to the silicon chip instead of attaching the silicon chip to another substrate.

3.1. Flip-chip techniques in electronic packaging

The best known of these techniques is perhaps solder bonding, originally developed by IBM in the 1960s. In solder bonding, some solder metal or metals are deposited on pads on the chip or the substrate or both and the chip is joined to the substrate by bringing the two together with careful alignment and under controlled temperature and pressure. There is a large number of variants in this technique, with various different solder metals, and various different preparatory metallizations of the pads on the chip and on the substrate to which it is to be bonded. The solder metals are usually soft (or "compliant") and have some thickness so that minor variations in height between different parts of the chip or substrate, or even warping of the chip or substrate, can be accommodated in the joining process. A typical thickness of the solder bump might be 50 μm, for example, though this number varies widely between different solder bonding techniques. Metals used for the soft "thick" solder include lead, tin, indium, and gold, often in alloys (for example, lead-tin). The softness and thickness of the solder metals are also important for accommodating the strain that results from the different thermal expansion coefficients of the chip and the substrate. Though the details of some of these schemes are publicly known, much of this technology is commercial practice. For a recent introduction and review see Lau.[30]

Fig. 1 illustrates a typical solder bonding process used in the packaging of a silicon chip to a substrate, shown here just before the completion of the actual bonding. The last layer above the aluminum bonding pad in the chip fabrication itself will typically be a glass passivation layer. An opening is formed in this layer over the aluminum pad region. Then various metals will be deposited. Typically, first an adhesion layer is formed, with a typical material being chromium. This layer may also serve as a barrier layer, or an additional barrier layer may be deposited. For example, in IBM's process, a mixed chromium-copper layer is formed to complete this adhesion/barrier layer. Then, a wetting layer, which might, for example, be copper, is deposited. Often, a final oxidation barrier layer is formed, typically of gold, to prevent the oxidation of the wetting layer. Finally, the solder metal is deposited, either by electroplating or by evaporation, onto this sequence of layers. The precise process that is performed on the substrate will depend on the specific substrate. The process could simply leave copper layers as the metals on the substrate, or more complex, multiple-layer metals could be formed just as on the chip itself. The final bonding process will bring the two parts, the chip and the substrate, together, possibly in the presence of a flux to remove oxides on the solder and the substrate metals, and possibly under pressure and high temperature. The solder may be reflowed during or after the initial bonding by heating above its melting temperature.

Various different-layer combinations have been reported for the metallizations on the aluminum pads on the chip, including chromium-copper-gold, titanium-tungsten-copper, titanium-copper, and titanium-tungsten-gold. Substrate metallizations include gold, copper, or copper-nickel-gold. Solders used include various lead/tin solders (all the way from eitectic 63% lead/57% tin, with a melting point of 183°C to 97% lead/3% tin, with a melting point of 310°C. Lead-indium solders have also been used in electronic packaging, as have indium-tin solders. Indium solder is often preferred for solder bonding to gold pads because of the low dissolution rate of gold in indium. Indium-tin solders appear to have longer lifetimes under thermal cycling than lead-tin solders.

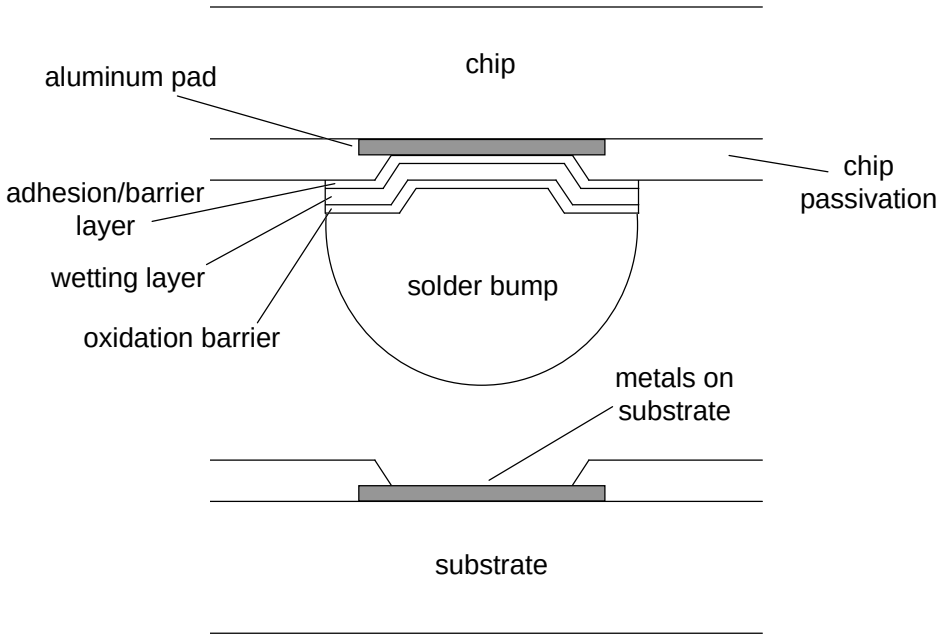

Fig. 1. Illustration of typical solder bonding technique used in flip-chip electrical packaging of a silicon chip to a substrate.

There are also various other approaches to flip chip attachment, including the use of short vertical wire bonds, conductive adhesives (both isotropic and anisotropic), and pressure contacts. Some techniques use flux to help remove oxide layers between the metals to be bonded. Elastomers have also been used between the bumps and the chips to give the desired compliance, and underfilling encapsulants are sometimes used between the chip and the substrate. Some techniques use reflow of the solder, i.e., melting the solder metal after joining the chip and the substrate. Because of the very large variety of these techniques, and because of the availability of other references in the literature,[30] we will not review these further here, and will concentrate on the specific examples of these and other techniques in optics.

3.2. Solder bonding in optoelectronics

Solder bonding is a technique that has already been extensively used in optoelectronics. The uses include the specific subject of this review, namely dense optical interconnections to silicon, as well as several other applications. It is worth briefly reviewing the other uses since they show some of the technical possibilities and options. After this, we will return to the specific subject of this review.

3.2.1. General use in optoelectronics

Solder bonding has been used to fabricate charge-coupled-device camera modules,[31] using both gold and indium alloy bumps, as well as an anisotropic conducting film technique. There is also some published work on the use of a chip-on-glass technique using gold and

indium-tin alloy bumps for repairable liquid crystal displays.[32] One of the major drivers for large-scale integration of optoelectronics to electronics through solder bonding has been the field of infrared imaged sensors.[33,34] Various of these infrared focal plane array technologies require the bonding of large numbers of optoelectronic detectors to underlying silicon processing technology. The dominant method for attaching the detectors to the silicon appears to have been indium solder bumps, perhaps because the indium, in addition to being soft and melting at relatively low temperature, also remains soft at the cryogenic temperatures required in the operation of many of these sensor systems. There appears, however, to be relatively little published literature discussing the details of these large-scale solder bonding techniques for detector arrays.

A completely different set of areas that requires solder-bonded detectors is in gamma-ray, x-ray, beta-radiography, and elementary particle detection. While not strictly optoelectronic in that the detected radiation is not optical, the technologies and dissimilar materials required are largely the same kinds as would be required for optoelectronic systems. In gamma-ray detection, for example, 48 × 48 arrays of CdZnTe detector pixels have been bonded on 125 μm centers, using indium, to a multiplexer chip.[35] 4 × 4 arrays of detectors have been bonded to CMOS for x-ray detection,[36] and 8 × 8 x-ray detectors with 150 μm pixels have been bonded to amplifiers and logic circuits for crystallographic detection.[37] 1024 silicon detector pixels have been bonded to electronics for beta radiography cameras,[38] and, in what may be the largest such solder-bonded integration of detectors and processing electronics, 288 CMOS readout chips have been bump-bonded to 48 Si detector matrices, assembled in 8 identical arrays for a total of nearly 300,000 pixel cells, with each 75 × 500 μm cell containing a complete set of signal processing electronics for use in elementary particle detection.[39]

The technology of solder bumping has also been applied in optoelectronics to the packaging of optoelectronic components with waveguide structures. A strong motivation here is to use the solder bonding to achieve the desired degree of alignment accuracy between the waveguides and the optoelectronics. By use of reflow, the surface tension in the temporarily-liquid solder metal can align the relative position of the two structures being bonded to a greater accuracy than the original attachment. Though some have claimed that very good alignment is possible, for example to within half a micron,[40] there is still some debate as to how precise such alignment can be.[41] Specific examples of such solder bonding include Au/Au thermo-compression flip chip bonding (i.e., bonded with heat and pressure, but without reflow) of optoelectronic devices to silicon motherboards for passive alignment,[42] a technique for integrating optoelectronic devices to multichip modules incorporating waveguide layers, with self alignment of the optoelectronic devices claimed within one micron through the use of microbump bonds,[43] integration of monolithic optoelectronic integrated circuit receiver circuits to a planar lightwave circuit,[44] other examples of flip-chip solder-bump bonding to a substrate containing electrical wiring and planar-processed optical waveguides,[45] and packaging of receivers to planar lightwave circuits.[46]

3.2.2. Solder bonding of arrays for dense optical interconnects

There has been substantial work in the bonding of arrays of optoelectronic devices to silicon integrated circuits using various versions of solder bump bonding. This has included work with quantum well modulator/detector (or SEED) arrays,[6-14, 47-52]

VCSELs,[53-57] and LEDs.[58,59] The published work on LED diode array chips includes bonding arrays with 75 μm diameter solder bumps on 156 μm pitch, with the resulting chips then being spaced 15 μm edge-to-edge, face down, on a glass substrate patterned with thin film metallization,[58] and bonding of LED and detector arrays to driver and receiver circuits.[59]

The recent interest in VCSELs as devices capable of operating in arrays has led to demonstrations, for example, of 1×64 microlaser chip indium-solder-bonded to a glass substrate,[53] and 16×1,[56] 6×6, [57] 8×8,[54] and 16×16 arrays solder-bonded to silicon circuits.[55] Individual VCSELs have also been bonded to silicon circuits through a solder bonding technique in which the substrate is removed by chemical etching. In this case, the bottom of the VCSEL is patterned with Pd-Ge-Sn dots, which are then bonded to gold pads on the silicon chip using a eutectic AuSn bond formed at 290°C.[60]

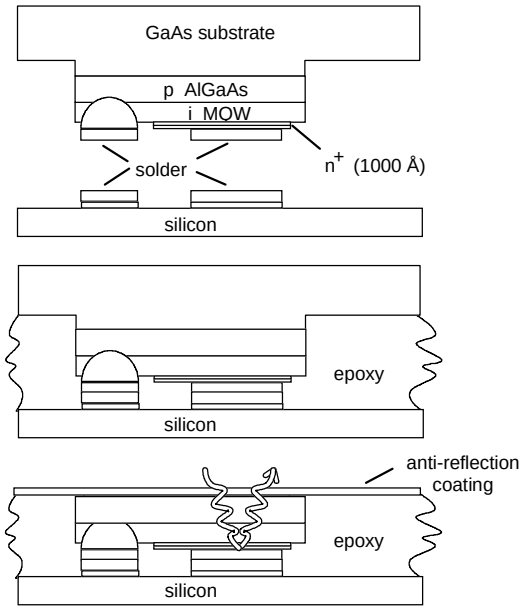

Fig. 2. Illustration of the process of bonding GaAs/AlGaAs quantum well modulator/ detector diodes to a silicon chip. After solder bonding the two chips, an epoxy is flowed between them, and the entire GaAs substrate is removed chemically, leaving the separate modulators bonded to the silicon chip. An anti-reflection coating is deposited, and the devices can be used as reflective modulators or as photodetectors. (After Goossen et al.[6])

Quantum well modulators have the advantage that it has been possible to make large arrays of these devices for some time, and they have seen the largest array bondings of any of the optical output devices. In some materials systems, the substrate on which the modulators are grown is transparent at the wavelength at which the modulators would be used. This is the case for modulators using InGaAs strained layers on GaAs substrates, and for essentially all modulator materials systems grown on InP (such as unstrained InGaAs). In this case with transparent substrates, it is straightforward to flip-chip mount these modulator arrays to silicon chips.[47,51]

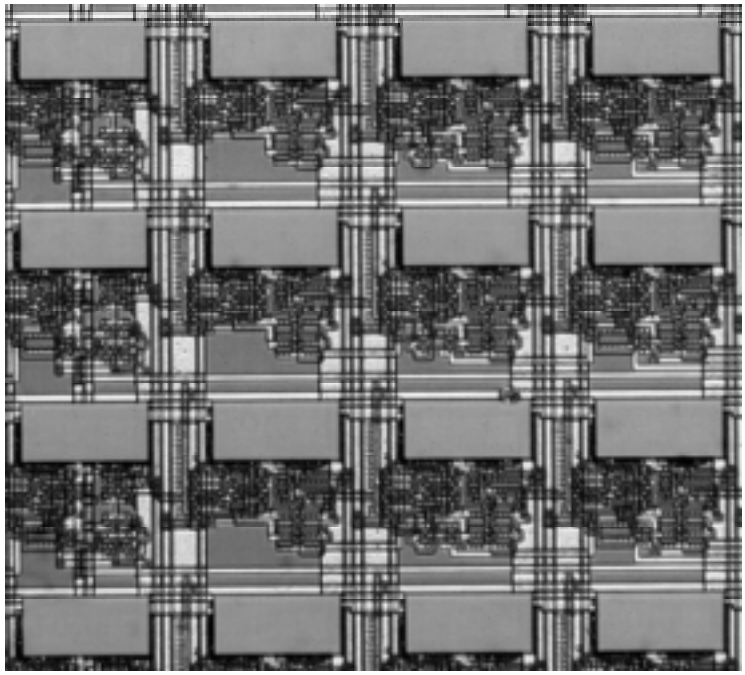

Fig. 3. Quantum well modulator/detector diode array bonded to a silicon switching chip.[11] The diodes are the rectangular regions, which are ~23-μm × 53-μm, and are located on 80-μm centers. The two solder bonding pads underneath the devices are 15-μm × 15-μm, with 15-μm spacing.

The material system that has the best performance for modulators, however, is the GaAs/AlGaAs system, in which the substrate is opaque at the desired operating wavelength (~850 nm). Goossen and co-workers[6] developed a technique for solder bonding these modulators, in which, after a thermo-compression solder bond, the space between the modulator chip and the silicon chip is back-filled with an epoxy, and then the entire GaAs substrate is chemically removed (see Fig. 2). Titanium-gold metallization was used on the quantum well diode pads, and titanium-platinum-gold metallization on the aluminum pads on the silicon chip, with lead-tin solder deposited on both metallizations. This technique has been demonstrated to very high yields, with successful bonding of over four thousand devices to a silicon CMOS chip.[11] The method has the great advantage that, because the substrate has been removed, the issue of thermal expansion mismatch between the compound semiconductor substrate and the silicon chip substrate is no longer important. Hence it is not necessary to use large solder bonds or very soft solder metals to allow for the thermal expansion mismatch. Worchesky and colleagues[52] have demonstrated arrays as large as 128 × 128 of uniform quantum well modulators using an indium bumping technique also to silicon chips.

Though detailed yield data is often not released for bonding processes, it appears in these cases that the yield for individual devices bonded and operating exceeds 0.999, meaning that bonding of fully-functional arrays of thousands of devices to silicon is quite feasible.

It may be at this level of yield that the yield limit is actually from the devices themselves rather than from the solder bonding process. These demonstrated results are therefore very encouraging for the successful attachment of many thousands of optoelectronic devices to silicon integrated circuits.

3.3. Other bonding techniques used for optoelectronic devices

3.3.1. Thermosonic bonding

Joining directly to pads without reflowing or melting the metal is possible by the use of high temperature to soften the metals and pressure to complete the joints, in which case the joint is referred to as a thermocompression bond. To make good joints, it may be necessary to use high temperatures or high pressures, neither of which may be desirable for a number of reasons. One well-known technique to alleviate these difficulties is to use ultrasonic energy as well. Such bonding is called thermosonic bonding, and is extensively used in attaching wires to chips. A great advantage of such a technique is that it does not require any additional metallizations on the aluminum pads on the silicon circuits. This technique has been extended to the bonding of arrays of devices,[61] and applied to bond 8×8 arrays of VCSELs to silicon chips, representing an additional practical option for such array bonding.

3.3.2. Compression microbumps

LED arrays were bonded to substrates on which silicon integrated circuits were also bonded by the same technique.[62] The technique used in this work involved micro bumps, and demonstrated linear arrays of 64 LEDs with bonds on 63.5 μm centers. The technique differs from conventional solder bonding in that the micro bumps are merely pressed onto the substrate contacts, but the chip and the substrate are held in strong compressive contact by a light-setting insulation resin between the chip and the substrate. This kind of technique allows multiple chips to be bonded sequentially to the same substrate. The same technique could be used to pitches as small as 10 μm with over two thousand bonds reliably formed. This technique also allows removal of the chips by dissolving the resin in a solvent.

3.3.3. Epitaxial lift-off

If an AlAs layer is grown as part of an epitaxial device structure, it is possible to etch away the entire AlAs layer to detach the entire epitaxial structure that was grown above the AlAs layer. This technique, pioneered by Yablonovitch et al.,[63] and recently reviewed,[64] is often referred to as epitaxial lift-off. It can be used to transfer entire devices or arrays of devices from their original substrate onto other "host" substrates. Transfer onto substrates as varied as silicon circuitry, polymers, glass, and lithium niobate has been achieved. An example of recent work includes the demonstration of the integration of an 8×8 array of thin-film GaAs-AlGaAs photodetectors onto a silicon array circuit.[65]

The method of bonding to the host substrate varies. Direct bonding, for example, of epitaxially-lifted-off GaAs devices to silicon, is possible through van der Waals forces that result from bringing the surfaces to be bonded into intimate contact, and this

technique is often used. A problem with this kind of technique is that the surfaces may not be flat enough for good bonding, though this can be approached by various processing techniques. 4×8 arrays of LEDs have been successfully bonded to silicon by this means.[66] If the host substrate is coated with palladium, a low-temperature reaction occurs, essentially through mechanical contact alone, which results in a robust, ohmic contact between the host substrate and the GaAs.[67] An approach that can solve the problem of the required flatness of the layer and host substrate, is to metallize the "bottom" of the devices, and connect these to electrical vias through an insulating, conforming, polyimide layer deposited on the silicon circuit.[68]

3.3.4. Wafer fusion

It is also possible to fuse wafers of dissimilar materials directly together. This technique has been used to make devices from such dissimilar materials. One such device, for example, is an avalanche photodetector with an InGaAs absorbing region and a Si avalanche region.[69] Such techniques can involve heating the wafers to relatively high temperatures (e.g., 650°C), and hence may not be as suitable for bonding to finished circuits. Such a technique can result in a covalent bonding between the materials. This process has been investigated in some detail.[70] Lasers have been bonded to silicon substrates using this technique.[71,72]

3.3.5. Polyimide bonding

Matsuo et al.[73] have developed a technique in which the epitaxial layers for optoelectronic devices are first formed on a GaAs substrate, which is then bonded using a polyimide layer to the silicon CMOS chip. The GaAs substrate is chemically removed, and then the photonic devices are fabricated in the epitaxial layers using conventional photolithographic processes. Holes are etched in the polyimide as necessary to allow electrical connections to the underlying silicon circuitry. Hybrid metal-semiconductor-metal (MSM) detector arrays were fabricated this way.

4. DEVICES

Thus far, we have discussed the technologies that can be used to bond arrays of optoelectronic devices to mainstream electronics. Here we will discuss the devices themselves and their suitability to the demanding tasks of dense, high-speed, interconnects to silicon electronics.

There are two different categories of devices required for optical interconnects — input devices (that is, photodetectors) and output devices (that is, emitters or modulators). There are important issues for all of these devices. They all, obviously, must be capable of being made in relatively large, dense arrays. It is also a reasonable requirement that the devices must be capable of operating at speeds as fast as those corresponding to the clock rate of the silicon circuitry itself. It is not likely that system designers will be enthusiastic about a technology that would require them to slow down the interconnects compared to the speed of the logic circuitry (though that is common practice with electrical interconnects today). It is also likely that, by the time dense optical interconnects are implemented commercially, the clock rates of silicon circuits will be

even faster than those currently in use; for example, a target of at least one to two gigahertz should be considered when contemplating optoelectronic technologies that would be usable for some substantial period of time.

4.1. Detectors

Detectors are, in general, substantially less of a problem than output devices. For optical interconnects, for example, both p-i-n detectors and metal-semiconductor-metal (MSM) detectors appear to be viable and practical solutions. In principle, silicon itself should be capable of being a good photodetector. Unfortunately, there are significant problems if we try to use silicon photodetectors made using CMOS processes for detection of the near-infrared wavelengths that suit the practical output devices. In practice, such CMOS detectors tend to be too slow. The core of the problem is that, for the near-infrared wavelengths where most output devices operate efficiently (e.g., 850 nm), silicon has a very long absorption length for the light (e.g., ~10 μm). This leads to the optical creation of carriers well outside the junction region of diodes formed in the silicon CMOS process. The resulting carriers can take a long time to diffuse back into the junction region where they eventually give rise to additional photocurrent. This can lead to very long tails on the response of silicon photodetectors (for an example of recent high-speed CMOS photodetector work, see Ayadi and Kuijk[74]). Also, the efficiency of such detectors for infrared light is poor because only a small fraction of the light gives rise to photocurrent directly in the junction region of the diodes. In practice, therefore, it seems that, at least for two-dimensional arrays of devices, the use of compound semiconductor photodiodes, with their strong, direct-gap absorption, and the flexibility to tailor the device structure for optimum operation through layered epitaxial growth, will be essential. Hence, the photodetectors will also have to be bonded to the electronic chips in some hybrid manner. With compound semiconductor photodetectors, there appears to be little problem with achieving speeds in the gigahertz range with good efficiencies.

4.2. Light-emitting diodes

The situation with output devices has been a much more difficult one, since, even with compound semiconductor technology, there was difficulty in getting output devices that could be made in sufficiently large numbers, with surface-normal operation required for two-dimensional arrays, and with power dissipation low enough for dense integration. An additional important issue that is sometimes overlooked is that, for efficient transfer of optical power from the output of one device to the input of another, it is highly desirable to use coherent (or, at least, diffraction-limited) light. The simplest and most readily fabricated light emitters, namely LEDs, do not produce diffraction-limited light.

Diffraction-limited light has a "minimum uncertainty" characteristic in that, for a given convergence angle of a light beam, the smallest possible focused spot will be formed. In practice, light that is not diffraction limited cannot generally all be collected and focused to a small spot. As a result, to operate a system without diffraction-limited light means that large photodetectors would have to be used to collect even a substantial fraction of the light from a non-diffraction-limited light source. The use of large photodetectors in turn means large photodetector capacitance, which in turn generally leads to a more difficult receiver design with, likely, higher power dissipation. Only lasers can

efficiently produce light with the property of being diffraction limited; this property is a natural consequence of the coherent generation of light inherent in the laser. The LED, however, is generally not coherent, and emits its light over a relatively large angular spread given the size of the LED itself. The efficiency of coupling light from an incoherent emitter, such as an LED to a small detector, can readily be as bad as 10^{-3}.

There are ways of approaching the issue of improving the efficiency of LEDs, such as the recent work using resonant microcavities and related techniques (see, e.g., Deneve et al.[75]), and such approaches may allow some use of LEDs in moderately dense interconnects. An additional problem with LEDs is that they may not be fast enough to handle the desired speeds. LEDs rely on intrinsic time constants, especially carrier recombination times, for their speed of response. If these times are shortened, the LED typically will become less efficient. Gigahertz speeds would represent a significant challenge for efficient LEDs.

There are also possibilities for light-emitting devices made in silicon technology,[76,77] with the recent work in porous silicon being particularly interesting. Porous silicon light emitters have been integrated with silicon circuitry.[78] Again, however, the problem is that, even if the silicon light emission is efficient, these devices are still LEDs and would have problems in making dense arrays for high-speed optical interconnects. The possibility of coherent light emission from a silicon-based technology still remains a basic research question.

4.3. Vertical-cavity, surface-emitting lasers

The most promising emitter for dense optical interconnects to silicon is the VCSEL. The conventional edge-emitting laser, though it can be made in two-dimensional arrays, and, with the use of integrated mirrors or other techniques, can be made to emit perpendicular to the surface, is not likely to be suitable for dense arrays simply because of the length of the cavity.

VCSELs have made substantial progress, and are the subject of intense research effort. There has been significant effort to demonstrate arrays of VCSELs.[79-89,53-57] Some of these arrays have been bonded to silicon circuitry, as discussed above.[53-57] Of these various arrays, some are quite large, with 144-element[86] and 100-element[88] arrays demonstrated, and a 64-element array, with all elements explicitly shown to be working, has been solder-bonded to a substrate (work on 256-element arrays[55] so far has apparently been concentrating on the flip chip process yield rather than demonstrating fully-operational arrays of bonded VCSELs).

Though VCSELs are attractive, and a number of moderately large arrays have been demonstrated solder-bonded to substrates, there are several outstanding issues for their use in dense optical interconnects. One major issue is the power dissipation of the VCSELs and the associated thermal effects. Though VCSELs may have low power dissipation compared to some common edge-emitting lasers, the power dissipation is far from negligible (it can reach ~300 W/mm^2 inside the device[90], actually higher than edge emitters), and can cause significant problems in trying to run entire, dense arrays of VCSELs at once. The thermal effects have been discussed by various authors, both

relating to thermal cross-talk between elements,[90-93] and to thermal time constants.[94-96] Many of the demonstrations of arrays of VCSELs turn on only one VCSEL at a time for these thermal reasons. Specific problems include overheating of the VCSEL (causing reduced power output, higher thresholds, and changes in wavelength of the VCSEL output), transient or spatially-varying thermal effects, such as microsecond time constants for settling of VCSEL operating characteristics,[94] and thermal lensing and self-focusing[90] that disturb the mode structure.

VCSELs can undoubtedly be modulated at very high speeds. For operation as dense interconnect devices, however, it is important that they can be driven with raw digital data, that is, data that does not have to be coded to improve its transmission. It is also highly desirable that the drivers for the VCSELs can operate from zero current rather than having to have a pre-bias current that is set close to the laser threshold. Any such coding, or pre-biasing that senses the laser threshold, would make the drive circuits more complex, inhibiting the use of VCSELs in dense arrays. If, however, VCSELs are driven from zero bias, there is a significant so-called "turn-on" delay — a delay between the start of the drive voltage pulse and the start of the emission by the VCSEL. This delay is caused by the time taken to build up sufficient carrier density inside the VCSEL to take the VCSEL above lasing threshold. Such delays can readily be hundreds of picoseconds. In addition to the issue of the delay itself, this delay is dependent on the preceding data, since the carrier density in the VCSEL depends on how long it has been since the VCSEL was last lasing. Hence, there is also a jitter caused by the turn-on delay in the VCSEL. Unless the VCSEL is deliberately biased close to threshold, which might require a feedback circuit to stabilize the bias (because of variability of thresholds from fabrication or temperature variations), the VCSEL may have to be driven approximately five or more times above its threshold current to give a low enough bit error rate.[97,98] VCSELs not running in a single mode also have additional jitter and intensity noise associated with mode competition.[98,99]

An important recent development has been the emergence of oxide-confined VCSELs.[100] A buried AlAs layer is oxidized in high-temperature water vapor from the outside of the VCSEL structure towards the center. This results in a narrow aperture inside the VCSEL, which both encourages current flow only through this aperture and also gives some index guiding for the mode. This therefore represents an attractive alternative to the proton-isolated structures that are currently the main method of fabrication of VCSELs in arrays. In these oxide-confined devices, low thresholds and high efficiencies can be obtained. The index guiding structure also helps reduce thermal lensing effects.[96] Small arrays have been demonstrated[81,82,84] up to 32 elements in size.[81] Such devices have not yet apparently been solder-bonded, and these structures are still relatively exotic compared to the more proven proton-isolated structures. They are, however, the subject of particularly active research.

4.4. Modulators

Modulators based on the quantum confined Stark effect[101] in quantum well diodes have been extensively investigated for use in two-dimensional arrays. The mechanism of the modulation has no speed limitations on the time scales of interest for optical interconnections. The physics of the electrical absorption effects is expected to remain

unchanged until sub-picosecond time scales.[102] The devices also do not have thresholds, and remain efficient down to arbitrarily low powers. In using modulators, the light beam arrays will be derived from lasers, and hence can readily be diffraction limited, so they do not suffer from the efficiency drawbacks of LEDs.

The issues with modulators for dense interconnection have included limited contrast ratio, moderately high drive voltage requirements, saturation, and the requirement that there be optics to generate and align arrays of light beams to the devices. The wavelength of the light must be chosen to match the modulators' optimum operating range, which typically requires specification and control within a few nanometers, and some degree of temperature stabilization (e.g., within 5-10 K variation) may be required for some devices. Despite these issues, many complex chips have been fabricated[9,10,11,12,14,16] and large systems demonstrated using large numbers of modulators.[20,21,51,52]

The issue of low contrast ratio (e.g., 3:1) has been addressed in two different ways. One method is to increase the contrast ratio by using asymmetric Fabry-Perot resonators (see, for example, Worchesky et al.[52]). By this means the contrast ratio can be substantially increased (e.g., 24:1 in arrays[52]), and devices made in large arrays.[52] Another method of handling the relatively low contrast ratio of simple modulators is to operate with pairs of modulators and pairs of light beams per channel — in other words, differential operation. This is the approach that has been taken in most of the digital systems made using modulators.[20-22]

In differential operation, the signal is a logic 1 if the first beam is brighter than the second beam, and is a logic 0 when the second beam is brighter than the first beam. The use of such differential signalling has many other advantages. It tends to give systems large dynamic range because there is no particular reference power at which the signal should be interpreted as a 1 rather than as a 0. It therefore makes the system independent of overall fluctuations in the optical power of the system. Differential operation also tends to make receiver design easier, especially since communication of logic levels without encoding requires that the system behave as if it were d.c. coupled. The differential operation means that it is not necessary, for example, to derive local reference voltages for the receiver from the average power of the incoming signal, a common receiver technique for "single-ended" (i.e., single beam) receivers, but one that makes it difficult to have a truly d.c.-coupled system that can respond all the way down to zero frequency. Differential signalling is now extensively used for high-performance electrical interconnects because of its many helpful features at the system level.

Simple quantum well modulators run well with bias swings of approximately 5 volts. This is compatible with current-generation silicon technology, but it is clearly desirable to reduce that for future generations. There are designs of quantum wells that allow lower-voltage operation, including, for example, asymmetric coupled wells[103]4and shallow quantum wells.[104] Even without changing the quantum well design, the simple technique of using two or more diodes optically in series and electrically in parallel can reduce the drive voltage requirement. For example, simply stacking two diodes one on top of the other leads to a halving of the drive voltage requirement.[105] It is also possible to stack multiple diodes and perform side contacting.[106] Such designs can also increase the operating wavelength and temperature range[106] (e.g., a temperature range of 25°-95° or a wavelength range of 15 nm). Another approach to the voltage issue is to use circuit

designs to give higher voltage swings for driving the modulators, a technique that should allow voltage drives substantially larger than the usual voltage supply in the logic circuitry.[107]

Saturation of absorption in quantum well modulators was an issue early on when the devices were operating as bistable switches that had to operate at the exciton absorption peak. Also, the early quantum well structures were not designed to minimize saturation. By redesigning the quantum wells, in particular by using thinner and/or lower barriers, the saturation intensity can be substantially increased. The saturation effect is reduced even further by arranging to operate at wavelengths beyond the zero-field band gap wavelength of the material; in this case, there is only optical absorption when there is a significant electric field across the quantum wells, and the created electrons and holes are swept rapidly out of the quantum wells by the field, preventing saturation. It has been shown that saturation intensities of >10 kW/cm^2 are readily obtained even at low electric fields, and much higher saturation intensities can be engineered if desired.[108-111] These high saturation intensities mean that there need be no saturation problems for quantum well modulators at the power levels required for optical interconnects.

Optics for the generation and manipulation of arrays of light beams for use with modulators have been shown under laboratory and system demonstration conditions many times.[20-22,112] Systems have worked successfully with more than 60,000 light beams.[112] While it is the case that some engineering effort would have to be devoted to make inexpensive, miniaturized, manufacturable optical systems for use with modulators, this would appear to be a feasible engineering task, and does not represent an insurmountable barrier to the introduction of modulator-based dense interconnection systems.

The ability to use one centralized laser to power the entire array of modulators is one that actually has significant potential system advantages. With a single laser source, it is necessary only to arrange for the wavelength and polarization stabilization of one laser. Quantum well modulators do require that the wavelength lie within an appropriate wavelength range, e.g., a few nanometers (though it has recently been shown[113] that, by merely varying the pre-bias voltage for the modulators, the usable wavelength range can be controlled over a 17 nm range, or, equivalently, a 60° temperature range). Such wavelength stabilization is also important for the use of diffractive optical systems and beam splitters for fan-out and complex interconnection patterns. A second advantage of centralized lasers is that clocking the single laser actually clocks the entire system automatically. It is also possible to use such centralized clocking actually to remove skew from signals in the system (see, e.g. Miller[3] for a discussion). By arranging the optical clock to be a relatively short pulse compared to the clock cycle, reading out the modulators with such an array of synchronized short-pulse beams means that the signal skew that went into the modulators is actually removed by reading out all of the modulators synchronously. Thus, in addition to their absence of turn-on jitter, modulators can actually reduce the jitter in the system.

4.5. Comparison of modulators and VCSELs

As discussed above, arguably the only two serious candidates at the moment for dense optoelectronic output devices for interconnection are quantum well modulators and VCSELs. The question then arises as to which of these is the better choice. Certainly, at

the present time, modulators are much more advanced than VCSELs in such applications. Not only have they been made and bonded in much larger arrays, but they have also been tested in real systems with large numbers of devices and light beams. Tests of VCSELs in systems have so far been limited to very small numbers of devices, and there is nothing to compare with the large multistage systems tested with modulator-based technology.

Given this more advanced state of modulator technology, the question is why go to VCSEL technology at all for dense interconnections? The answer to this question is by no means clear. The most commonly voiced criticism of modulators is that they need additional optics to bring the arrays of light beams to the modulators, and some control of laser wavelength is required. It is a matter of opinion (and some debate) whether this is a more serious problem than the many other problems that would have to be addressed before VCSELs might be a viable solution at high densities. Such problems with VCSELs include many issues discussed above, such as power dissipation, and timing issues. VCSELs can only make the timing in the system worse, whereas modulators could actually improve the system timing.

Modulators and VCSELs can certainly be compared in terms of simple performance metrics, such as power dissipation. There have been at least two such studies[114,115] (the study by Fan et al.[114] also compares another possible modulator option, based on PLZT devices). The general conclusion from such studies is that modulator- and VCSEL-based systems would have comparable power dissipation overall when running at high clock rates (for example, greater than one gigahertz), and modulators would have better power performance at lower rates. The primary reason for the higher power dissipation at lower clock rates for VCSELs is that they are threshold devices.

Both of these studies take a very conservative view of saturation in modulators, presuming the modulator saturation intensity is about 1 kW/cm^2; in fact, it is at least 10 kW/cm^2 in well-designed devices, and can readily be engineered to be much higher, as discussed above. Hence in the study by Fan et al.,[114] where it is concluded that the modulator area will have to increase when running systems at high speed to avoid saturation, the power dissipation of modulators at high speeds may be overestimated. In the study by Nakahara et al.,[115] this conservative view of saturation problems in modulators leads them to conclude that modulators cannot be used at switching speeds faster than 300 ps, a limit that can, therefore, likely be surpassed.

The studies also do not analyze in any detail the penalty to the system from the additional jitter and unpredictability of timing in VCSEL-based systems if they are to be run with zero bias. In order to overcome these jitter phenomena, it may be necessary to drive the VCSELs even further above threshold, thus increasing the power dissipation of the VCSEL systems. Nakahara et al.[115] assume the VCSELs will be biased near threshold, but the cost of the necessary additional circuitry to control this bias is not included in the analysis.

Modulators have other incidental advantages. Because the same device can be used both as an efficient modulator and as an efficient photodetector, it is not necessary to have two different kinds of devices bonded in the system, a considerable simplification of manufacture. VCSELs, by contrast, are not generally good photodetectors, and hence a separate photodetector has to be created for the system. With modulators, the same diode

could be used as both a detector and a modulator.[116] Modulators can be used quite effectively even with short optical pulses as the optical power source. Short pulses allow more efficient receiver circuits.[117] It is also possible to consider advanced concepts such as wavelength division multiplexing of interconnects. This could, in principle, be done with either modulators or arrays of lasers. In the case of arrays of lasers, the different lasers have to emit at carefully-controlled wavelengths. In the case of modulators, the same modulator can work over relatively broad ranges of wavelength, and hence does not have to be tuned to the specific wavelength desired for each channel of the interconnection. One experimental system uses short optical pulses to generate multiple wavelengths,[118] allowing interconnections of many channels over one fiber while also getting the further advantages of short optical pulses for synchronization, receiver performance improvement, and clock phase recovery.

It is sometimes argued that it is difficult to align beams to modulators. It would, however, seem to be equally hard to align VCSELs with the optics required to handle the arrays of light beams from the VCSELs. In fact, low-power VCSELs are liable to have smaller light beams than are required to run modulators, so the alignment might even have to be more carefully controlled in the VCSEL case. In the alignment of beams with modulators, it is not necessary that the beam hit the middle of the modulator, so the actual alignment of the modulators to the beams can be relatively relaxed. One final point that is relevant in particular to solder bump bonding is that, with modulators, it may be possible to grow the devices on silicon substrates.[119] This might allow the bonding of modulators to silicon CMOS circuits at the wafer level, because there would be no thermal mismatch between the silicon circuit substrate and the modulator array silicon substrate at the time of bonding. The thermal expansion mismatch is one of the limits to the size of compound semiconductor device arrays that can be bonded at one time onto the silicon substrate.

5. CONCLUSIONS

There is a strong rationale for considering dense optical interconnects to silicon; such an approach takes advantage of many features of optics that are weaknesses of electrical interconnects, while giving up none of the strengths of silicon logic technologies. Though, in the future, monolithic integrations of optoelectronic devices and silicon electronics may be possible, hybrid techniques, allowing silicon and optoelectronics to be fabricated and optimized separately, are attractive for introducing such combinations of optoelectronics and silicon.

It is clear from the discussion here that hybrid techniques for bonding optoelectronic devices in large numbers to silicon integrated circuits can work very well, both in terms of the numbers of devices that can be bonded and in the performance of the bonded systems (e.g., low parasitic capacitance). There are many different techniques for bonding. Solder bonding in particular has been demonstrated to be very flexible and have high yields.

There are also promising device technologies for very high density optical interconnections. Detectors for appropriate input devices appear to present no basic problem, though likely they will also have to be compound semiconductor devices. For output devices, quantum well modulator arrays already have been demonstrated to work well in large hybridized arrays, and have been successfully tested in large system

demonstrators. VCSELs may ultimately achieve performance comparable to modulators at high speeds, though issues remain with timing jitter, driving circuits, power dissipation, and demonstrated yield of large arrays; the rationale for replacing modulators with VCSELs is not clear, especially given other qualitative benefits of modulators in large systems. The use of oxide-confined VCSELs may be essential to get good-enough performance for any dense interconnects based on VCSELs. Another important issue for VCSELs is that they have not been tested in large system demonstrations, which makes comparison to the more advanced modulator technology difficult.

Regardless of the device and bonding technology, a considerable weakness in all dense optical interconnect systems is the lack of sufficiently developed optical technology for inexpensive, miniaturized, and convenient handling of arrays of light beams. Both VCSELs and modulators require good alignment of the optical systems, at least at the interface to the devices themselves (e.g., within 10 μm, or possibly better for low-power VCSELs). There does not appear to be any fundamental mechanical difficulty in designing such systems, and large systems have been demonstrated in the laboratory. It is likely possible to use lithographic techniques to align the most critical parts (e.g., lenslet arrays to the device arrays), with comparatively relaxed tolerances elsewhere. "Snap-fit" array optics, for interfacing to two-dimensional array devices and for local free-space parallel-array connections, and highly parallel flGxible fiber ribbons or bundles for longer connections, are likely more critical issues now for implementing dense optical interconnections than are either the device or hybrid integration technologies.

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