

# High-Impedance High-Frequency Silicon Detector response for Precise Receiverless Optical Clock Injection

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## ABSTRACT

We report the direct injection of precise clock signals into standard CMOS circuits using short optical pulses by a novel receiverless scheme that eliminates the delay, skew and jitter of a typical receiver. To accomplish the optical injection we designed small silicon detectors along-side standard  $0.25\mu\text{m}$  CMOS-circuits. Due to the low intrinsic capacitance of the detectors, the photogenerated carriers can directly generate voltage swings that are comparable with CMOS voltage levels if the detectors are loaded with high-impedance circuits.

As a first step to implement this scheme we characterized various detectors built in the CMOS process for their high-frequency response. In a test set-up the silicon detectors are sampled with on-chip samplers that only present a small capacitive loading to the detector node. We present the high-frequency high-impedance response measured with this scheme together with capacitance measurements and DC responsivities of various types and sizes of detectors. The characterized long tails typically observed with silicon detectors allowed us to set up a model for the power penalty we have to take into account for precise clock detection.

Finally, as a proof-of-principle demonstration we present the first results of this receiverless scheme in which a totem-pole of silicon detectors directly drives an on-chip CMOS inverter.

**Keywords:** Silicon Detectors, CMOS, receivers, on-chip samplers

## 1. INTRODUCTION

Since the invention of the integrated circuit (IC), the electronics industry has been trying to integrate as many functions as feasible onto one chip. This idea, driven by the economies of scale, has proven to be most successful for CMOS technology. The Semiconductor Industry Association predicts this increasing integration will continue in the coming decade. The quest for integration of optical communication functions in this technology appears, however, to be a more difficult task. The improvement of both hybridization techniques<sup>1,2</sup> and the attainable clock speeds have only recently turned CMOS technology into a viable candidate for optical communication at gigabit/s rates.

Optics by its nature can also improve the capabilities of a CMOS chip.<sup>3</sup> There has, for example, been a large effort to create optical signal I/O's to alleviate the growing bottleneck for off-chip communication.<sup>1,4</sup> The need for precise clocks has also resulted in several attempts to distribute clocks optically inside systems.<sup>5,6</sup> In this work we build very small detectors, which we use to optically trigger specialty circuits on the chip, with a range of time-critical applications in mind.

The receiving end of an optical link typically consists of a detector and an electronic receiver circuit. The detector is optimized to efficiently convert impinging photons into an electric current signal. The receiver circuit will then amplify the photogenerated current into a large signal suitable for standard digital logic.

The input stage of the receiver circuitry generally consists of a transimpedance amplifier or a clocked sense-amplifier. Both topologies prefer a detector with minimal capacitance, since a given number of photogenerated

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carriers at the detector will then induce a large voltage swing at the input. In this work we push this idea one step further: we scale down the size, and hence the capacitance of the detectors such that an optical signal can directly generate large enough voltage swings to drive logic inputs directly from the terminals of the detectors with appropriate optical power levels. In this scheme we do not require any receiving amplifier circuit at all, and therefore are eliminating the delay, skew and jitter a normal receiving circuit would introduce. This idea leads to the concept of *receiverless* data injection.

We can also use the high-frequency nature of optics for synchronization, an important function in clocked systems. In contrast to electronics, it is relatively straightforward in optics to generate extremely short-pulses (on the order 100fs to 10ps) using the technique of mode-locking a laser.<sup>3,7,8</sup> The repetition rate is solely defined by the round trip time in the laser, making the generated pulse stream a very stable clock source. It is also relatively easy to propagate these pulsed signals optically inside systems using conventional off-the-shelf optical components. These characteristics lead us to believe that the proposed receiverless scheme can not only be used to create optical links but also, by taking advantage of the properties of optical short pulses to trigger circuitry with very precise clocks.

The generation of precise clocks is crucial in today's high-speed integrated circuits. In fact, the accuracy of clocks is in most cases the limiting factor in multiplexing systems or any system where high-frequency time-critical conversions have to be applied. For example, the time resolution of a NMOS sampling switch in a standard  $0.8\mu\text{m}$  CMOS-technology has been estimated to be 21ps (48Gb/s) when no jitter is considered on the clock at the switch,<sup>9</sup> while in practical systems the attainable speeds are much slower primarily due to the low accuracy of the clocks. By combining the idea of receiverless data injection and the synchronization advantage of optical short pulses we arrive at the concept of *receiverless clock injection*.

To accomplish this receiverless optical injection we monolithically integrated silicon detectors on standard  $0.25\mu\text{m}$  CMOS chips. We selected this approach not only because silicon detectors can be easily integrated at very low cost in standard CMOS circuits, but also because they do not have the fringe capacitance a hybrid integration technique would introduce. The detector is directly connected to the gate of transistors, so it is only loaded by a small capacitance, allowing a large signal to be integrated on the detector by the photogenerated carriers. Using this scheme we can optically trigger time-critical specialty circuits. As it is relatively easy to fabricate low-cost sources in the near infrared spectrum we will work with a nominal wavelength of 850nm.

It is generally known that silicon is not the most preferred material for making fast photodiodes for the near infrared. In section 2 we take a closer look at the properties of silicon detectors at these wavelengths. In section 3 we present the DC responsivity and capacitance measurements of our devices. Section 4 proposes the use of a new scheme for characterizing high-speed signals in a detector: the use of on-chip samplers for high-frequency-content analog signals. This technique is applied in section 5 to determine the high-impedance frequency response of the silicon detectors. Finally, a first proof-of-principle operation of receiverless optical injection is demonstrated in section 6.

## 2. SILICON DETECTORS

Due to the indirect nature of the silicon bandgap, the absorption coefficient ( $\alpha$ ) has only a gradual onset behavior with the photon energy of the light, in contrast to direct bandgap materials, which has a much more abrupt absorption profile near the band-edge. This results in a rather poor absorption at the wavelength of our interest, 850nm.<sup>10</sup> The absorption length ( $1/\alpha$ ) is estimated to be  $14\mu\text{m}$ , i.e. light will penetrate much deeper into the substrate compared to the vertical diode lengths possible in current standard CMOS technologies. The  $0.25\mu\text{m}$  technology we are using in this work has, for example, a nominal n-well depth of  $1.2\mu\text{m}$ .

Thus, only a small fraction of the light is absorbed directly in the thin depletion region of the diode formed by the n-well or highly-doped diffusion areas. Most of the light penetrates deeper into the substrate and generates photocarriers. Some of these photocarriers will diffuse upward and finally be captured in the diode at the surface. This means that the detector will have to rely heavily on the diffusive transport of the photogenerated carriers in the substrate. As the diffusion transport is essentially a random walk, it can take a long time for the deep carriers to diffuse out completely. Consequently the monolithic integrated silicon detectors are mostly

plagued with a long tail in the response or a low-frequency gain, which makes it less straightforward to use them at high speeds.<sup>11</sup>

As this low-frequency response is driven by diffusive transport, however, the frequency response will not fall as a normal first-order system. To gain insight into this behavior we studied the diffusion equation. The number of excess minority carriers at a point in the p-substrate is the difference between the actual minority carriers and the equilibrium level<sup>12</sup> ( $n = n_p - n_{p0}$ ). The diffusion equation for the excess minority carrier concentration is as follows:

$$D \frac{\partial^2 n}{\partial x^2} - \frac{\partial n}{\partial t} - \frac{n}{\tau_p} = 0, \quad (1)$$

If we neglect the finite minority carrier lifetime ( $\tau_p \rightarrow \infty$ ) and perform a Laplace transform in time on the minority carriers<sup>13</sup>

$$\tilde{n}(x, s) = \int_0^\infty e^{-st} n(x, t) dt, \quad (2)$$

the diffusion equation becomes

$$D \frac{\partial^2 \tilde{n}}{\partial x^2} = s \tilde{n}, \quad (3)$$

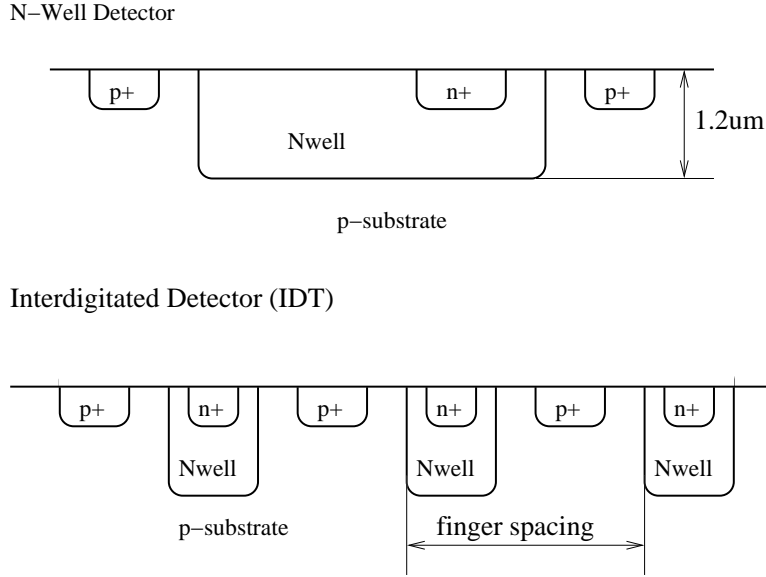
The solution of this ordinary differential equation is of the form:

$$\tilde{n}(x, s) = A(s)e^{-x\sqrt{s/D}} + B(s)e^{+x\sqrt{s/D}} \quad (4)$$

This suggests that the frequency behavior of the minority carriers concentration depends on the square root of  $s$ . Although the complete problem of the current response cannot be solved analytically, we do get a hint that the response will behave with the square root of the frequency and not fall off as a normal first order system. Thus, although the notion of the 3dB bandwidth of such a device is a property that can be measured, it does not have the same implications as is does in a linear system with only one dominant pole. In our work we experimentally prove that the frequency response of the detectors has indeed a sub-20dB/decade response.

The devices will eventually be used in a receiverless scheme, and thus will only be connected to a few gates of transistors, representing a small capacitive load. Using on-chip samplers, which we will explain in section 4, we are able to create a similar loading while characterizing the detectors.

In this work, we have used two types of silicon detectors which are shown in the cross-section in figure 1. The first detector consists of the horizontal diode formed by the n-well and the p-substrate. The second type of detector has interdigitated p-diffusion and n-diffusion areas contained within an n-well. The n-diffusion serves to lower the conductance of the layers, while the lower doping of the n-well decreases the capacitance. The anode and cathode fingers of the interdigitated device are connected by metal layers. Interdigitation is employed to form lateral diodes as well as vertical diodes to maximize the depletion region in the device. For each topology we implement two detectors with slightly different dimensions, as summarized in table 1. The second interdigitated detector also has metal lines above the n-well regions, which will increase the ratio of the carriers captured directly by the lateral diodes to those photogenerated carriers that diffused up from the substrate.



**Figure 1:** A cross-sectional view of the two silicon detector topologies.

**Table 1.** The dimensions and the capacitance of the silicon detectors implemented in this work. Two n-well detectors and two interdigitated detectors of different size were chosen.

	Area	Finger spacing	Capacitance
Nwell Detector 1	$10 \times 11.6 \mu\text{m}^2$	/	30fF
Nwell Detector 2	$20 \times 21.6 \mu\text{m}^2$	/	85fF
Interdigitated detector 1	$19.2 \times 20 \mu\text{m}^2$	$4.4 \mu\text{m}$	122fF
Interdigitated detector 2	$22.4 \times 20 \mu\text{m}^2$	$5.2 \mu\text{m}$	124fF

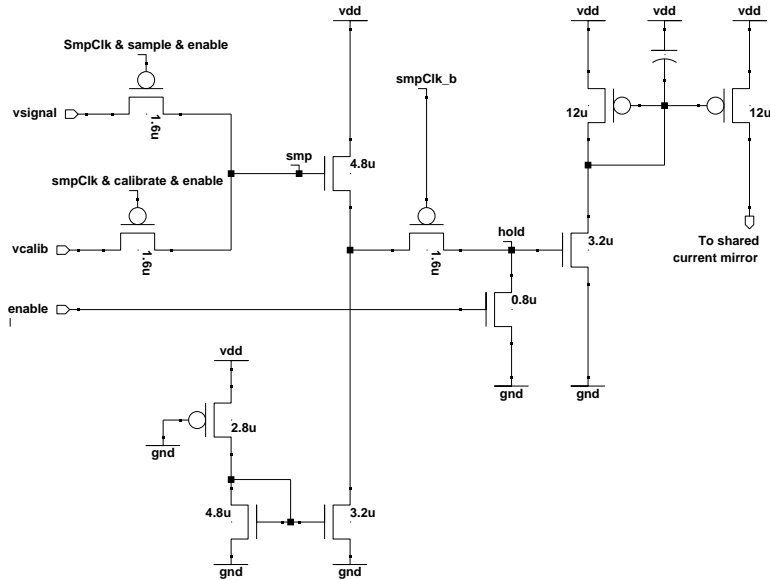
### 3. CAPACITANCE MEASUREMENT

We are mainly interested in measuring the high-impedance frequency response of the silicon detectors. We have also, however, characterized the DC-responsivity and made a measurement of the capacitance for completeness. The DC-responsivities, measured by an optical probe-station set-up, all range between  $0.025 A/W$  and  $0.03 A/W$ .

We measured the on-chip capacitance of the detectors using on-chip ring oscillators. The capacitance measurement was realized by comparing the frequency of an unloaded ring-oscillator to the frequency of the same oscillators loaded by the detectors.<sup>14</sup> The oscillators used consist of a 5-stage inverter ring. The maximum current in the inverters is controlled by means of an external bias voltage. Every node is loaded with a copy of the silicon detector whose capacitance is being measured. The frequency of the inverter stage is divided by 32 before it is extracted electrically. The resulting capacitances are shown in the last column of Table 1.

### 4. ON-CHIP SAMPLERS

In section 2 we touched upon the need for characterization of the frequency behavior of silicon detectors. This section will propose a technique to accurately measure this response. The detectors used in our approach will eventually only be loaded by a small capacitive load, i.e. the gates of only a few transistors. Therefore, to expose the silicon detector to similar environments while in characterization, we decided to integrate on-chip samplers.



**Figure 2.** The circuit schematic for the on-chip sampler in  $0.25\mu\text{m}$  CMOS-technology. All transistors sizes have a minimal length.

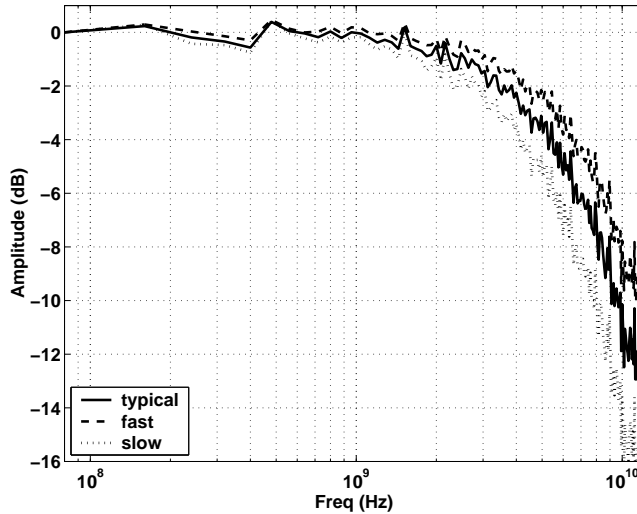
On-chip samplers make it possible to measure analog signals that have relatively high-frequency content inside chips. This technique was previously proposed by Larsson and Svensson<sup>15</sup> in 1993. The idea of on-chip samplers relies on the high bandwidth of MOS transmission gates. By subsampling repetitive analog signals with a slightly different clock, we can reconstruct the behavior of analog high-speed on-chip signals.

The core of the on-chip sampler circuit is a master-slave sample-and-hold switched capacitor circuit,<sup>16</sup> as shown in figure 2. The charge sharing between comparable sample and hold capacitance imposes a bandwidth limitation as predicted in switched capacitor network theory. Therefore a source-follower buffer is placed between the master and slave nodes (marked by *smp* and *hold* on the schematic). The hold voltages are then transformed into a current signal that can be easily extracted from the chip. Moreover, the current output makes it possible to multiplex the output of several on-chip samplers together. We use a scan-chain to select one sampler at a time. This technique reduces the number of pins needed to a total of six, independent of the number of implemented samplers.

Since the relation between the sampled voltage and the output current is not linear and depends on transistor parameters, we have provided every sampler with a calibration feature. We can independently calibrate every sampler by sampling a slow sweep of an external bias voltage on the *vcalib* terminal. The transmission gates of the samplers consist solely of PMOS transistors; therefore it is only possible to measure signals above threshold ( $\sim 1.1\text{V}$ ).

The samplers were externally clocked by a dual-channel pulse generator (HP8133A) that is locked at the pulsating frequency of a short pulse mode-locked laser. The pulse generator also has a delay feature by which it can introduce a known delay between its channels. To sample on-chip signals we have written a program that scans the delay of the sampler's channel while measuring the output current.

We extensively simulated the speed at which the on-chip samplers are expected to work. This is not a straightforward task due to the large difference in time-scale between the output of the samplers and the frequency spectrum at the input node. In order to get the frequency response within a reasonable time frame, we have created a broadband input signal having equal amplitude frequency components from 80Mhz up to 16Ghz with a low peaking in the time-domain. The low peaking property, important to minimize the non-linear effects, was optimized by repeatedly shifting the phases of the components through a stimulated annealing technique.



**Figure 3:** Simulation of the frequency response of the on-chip samplers for a slow, typical and fast process corner.

The resulting signal was then fed to the on-chip samplers by a data-driven spice simulation. Figure 3 shows that the resulting frequency behavior has a 3dB bandwidth of about 4Ghz.

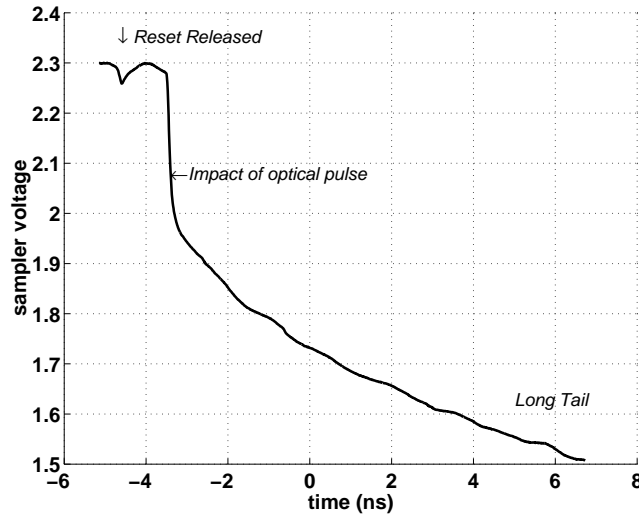
The output of the sampler settles on a much smaller time scale than the pulsation period of the short pulse laser. This allows us to extract even more information from the sampled signal by connecting the sampler’s output to a high-speed oversampling oscilloscope. The oversampling oscilloscope in itself constructs the trace by consecutively sampling different periods of the real signal. Thus, by acquiring the oscilloscope’s whole signal, we actually get several versions of the sampled signal. This allows us to estimate the noise in the sampled signal for a certain delay. A complication of this technique is that the samplers’ output is contaminated with clock feedthrough at the slave switch. This can be compensated by calibrating the ripple beforehand for different output currents. The technique presented in this paragraph is used in section 6 to measure the jitter of the injected clock signals.

## 5. HIGH-IMPEDANCE FREQUENCY RESPONSE

In this section we combine the samplers with the silicon detectors. The voltage signal created by an optical short pulse is sampled directly on the chip for several detectors. The short pulses are generated by a mode-locked Ti:Sapphire laser with a repetition rate of 82MHz. The pulse-width is about 100fs, which is much smaller than all time scales encountered on the chip. We are thus measuring a good approximation of the impulse response of the detector.

To make the signal periodic, we reset the detector to the supply rail every period by means of a pass transistor. We align the clocks such that the optical pulse is incident a short time after releasing the reset. One can see a typical sampled trace depicted in figure 4. The small glitch at the start of the plot is due to the release of the reset on the detector node. After a short while the optical pulse is seen to impinge onto the detector, resulting in a fast rising edge followed by the typical long tail response.

At the arrival of a pulse, the photogenerated carriers start to diffuse into the diode depletion region. These new charges result in a voltage change within the detector, which is inversely proportional to the capacitance of the device ( $CdV/dt = i(t)$ ). By taking the derivative of the sampled voltage in time, we are calculating a signal that is proportional to the photogenerated current, assuming the capacitance remains constant. Applying the Fourier transform will provide us with the frequency behavior of the silicon detectors. The response is shown for the different silicon diodes in figure 5. The traces were normalized with respect to the first frequency component



**Figure 4.** The sampled signal trace showing the response of the first interdigitated detector to an optical short-pulse. The optical energy in the pulse is  $0.74pJ$ .

for comparison. The curve of the second interdigitated detector, which was very similar to the first one, is not shown for clarity.

The plot clearly shows that the frequency response upto at least 2 GHz falls off with a sub-20dB/decade response, which indicates that the silicon detector cannot be modeled as a simple first-order system. In fact the response falls off by about half of what is expected for a first-order system, suggesting that we can model the response with a similar model:

$$\rho(s) = \frac{1}{1 + \sqrt{s\tau_a}}. \quad (5)$$

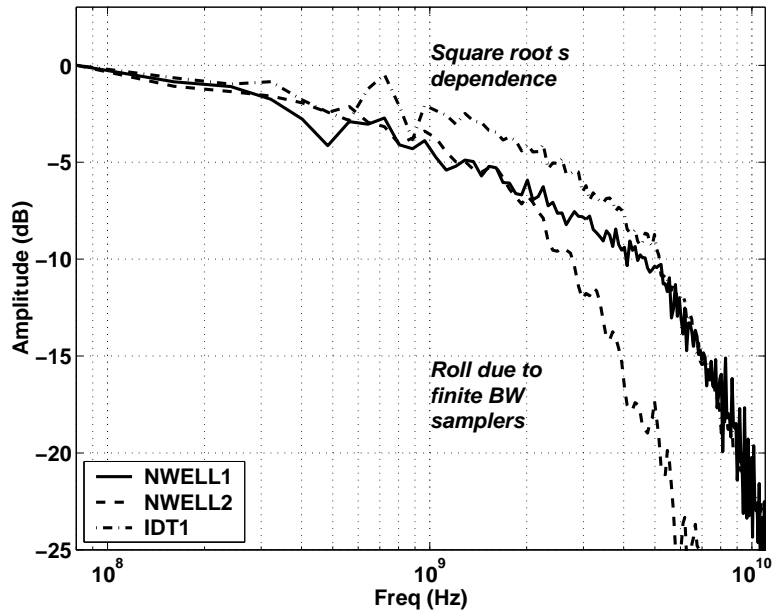
With this set-up it is hard to estimate the time-constant,  $\tau_a$ , of the device, because this constant is smaller than the lowest frequency component we are measuring, namely 82Mhz, the repetition rate of the optical pulses.

As simulations have predicted, the frequency plot falls off more rapidly when we cross the 4Ghz edge: we are working above the bandwidth of the on-chip samplers in this regime (section 4).

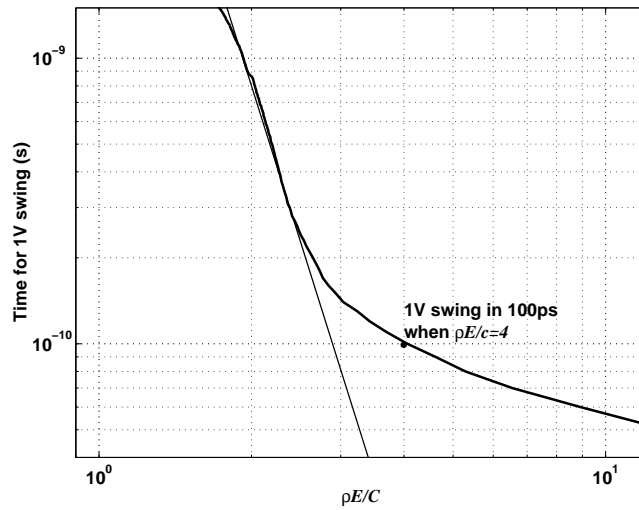
To get an estimate of the minimal power needed to create a 1V swing for a certain time delay, we included figure 6. The curve is the same as figure 5 but it has now been normalized by the capacitance and DC responsivity of the detector. The abscissa of the logarithmic plot is expressed in units of  $\rho E/C$ . If one injects an optical pulse of energy,  $E$ , into a similar silicon detector with a known DC-responsivity,  $\rho$ , and capacitance,  $C$ , one will get a voltage swing of 1V on the diode after a delay given by the curve. The value of  $\rho E/C$  is, at the same time, the voltage swing one will create with this pulse after an infinitely long time.

The curve follows more or less a straight line until a delay of about 100ps. For smaller delays the finite bandwidth of the on-chip samplers becomes a limiting factor. Nevertheless, if one injects an optical pulse with a value of  $\rho E/C$  of about 4, one will create a 1V swing on the chip in less then 100ps. This also means that we will have to inject pulses with four times more energy as required to get the 1V swing in an infinite long time.

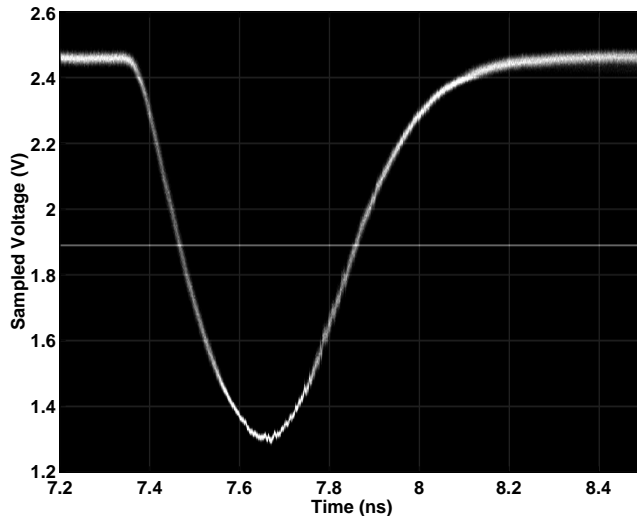
It is worthwhile noting that this sub 20dB/decade behavior favors our receiverless scheme with silicon detectors. Indeed, even if we use the silicon detectors above their 3dB bandwidth, a large amount of response is still available because the frequency behavior is falling off less rapidly than a normal first order system.



**Figure 5.** The frequency behaviour of the various silicon detectors. The response of the second interdigitated detector was not included for clarity. The curves have been normalized in respect to their first frequency component for comparison reasons.



**Figure 6.** The logarithmic plot shows the time it will take for an optical pulse of energy  $E$  in a detector with DC-responsivity  $\rho$  and capacitance  $C$  to create a 1V swing. For values below 100ps the results are limited by the finite bandwidth of the sampler. The value of  $\rho E/C$  also corresponds to the swing the pulse will create after an infinite long time.



**Figure 7.** Receiverless optical clock injection with optical short pulses of  $6\text{ pJ}$  onto the totem-pole configuration of interdigitated detectors. For given coordinates of a point on the gray-scale image the intensity is proportional to the the probability of a sample at that point.

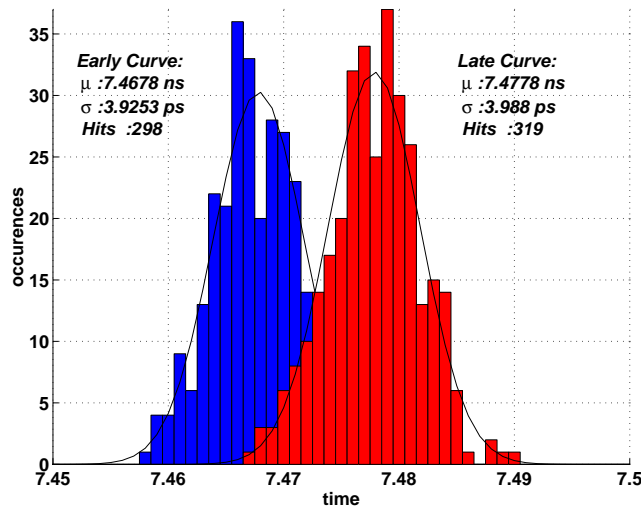
## 6. RECEIVERLESS OPTICAL CLOCK INJECTION

In this section we present a proof-of-principle demonstration of receiverless precise clock injection. We implemented the receiverless scheme by connecting tiny silicon detectors in a totem-pole configuration on the chip. The top diode, connected to the supply, is used to inject a rising edge. The bottom diode, connected to ground, can be used to reset the voltage back to its initial ground state. By alternating pulses on both detectors we are able to inject a precise clock onto the chip. In our case, the totem-pole configuration of detectors is connected to a small digital CMOS inverter. The signals at the output of this inverter are then sampled with the on-chip samplers as has been explained in section 4. Since the size of the silicon detectors was designed to be even smaller for this demonstration, we have chosen to sample at the output of the inverter rather than at the detector in order to minimize the distortion of the signal. If necessary, we can also set the node of the detector to an externally supplied bias through a minimum-size pass transistor.

Two different copies of this scheme were implemented on the chip. In a first copy we created a totem pole out of a n-well/p-substrate detector with a p-diffusion/n-well detector at  $5\text{ }\mu\text{m}$  spacing. Due to the strong difference in responsivities between the two detectors and due to the diffusion of carriers from one detector to the other, we were not able to create any significant swing on the device. In future designs we will increase the distance to solve this problem.

The second design was implemented with interdigitated detectors. The two detectors have two very small fingers resulting in a  $14.4\text{ }\mu\text{m} \times 10.4\text{ }\mu\text{m}$  detector area. Unfortunately this also created a substrate connection, tying the detector node to ground. On one hand this makes the scheme self-resetting such that we can inject clock-pulses with only one beam. On the other hand, however, the substrate connection demands more power. Figure 7 shows the sampled output of the inverter when a pulse of  $6\text{ pJ}$  is incident onto the device. Assuming a substrate contact resistance of about  $600\Omega$ , the curve is very similar to what simulations predict. These simulations also show us that the slew-rate of the curve is primarily limited by the inverter.

Figure 7 is a gray-scale image where, for given coordinates, the intensity of a point is proportional to the probability of a sample. The image was created using the technique explained at the end of section 4. We subsequently cut the rising edge at half of the swing. In this way we obtain a histogram with a shape as depicted in figure 8. The standard deviation of the jitter is close to  $4\text{ ps}$  and we obtain a peak-to-peak jitter of



**Figure 8.** Histogram of the pulse signals crossing at marker level at half their swing. The histograms correspond to two experiments one of which is delayed 10 *ps* more compared to the reference clock.

20 *ps*. These jitter results match well with the accuracy of the set-up: when we measure optical pulses directly with the high-speed oscilloscope, we obtain a similar jitter with standard deviation of 3.7 *ps*.

Using a translation stage it is very easy to precisely control the time at which an optical pulse impinges on the device. This is illustrated quantitatively in figure 8, where we have plotted the jitter histogram of two curves, one of which is delayed by 10 *ps* with respect to the reference clock. The mean of the rising edge is shifted in time by exactly 10 *ps*, proving the accuracy of the technique.

In this proof-of-principle demonstration, the detector node drives an inverter. However, since the sampled signal is at the output of the inverter and not at the detector, we are not only measuring a less sharp rising edge, but also measuring the jitter added by the inverter. Consequently, we can assume that the signal at the detector side might perform even better.

## 7. CONCLUSIONS

In this work we have introduced the concept of receiverless clock injection. The technique involves receiverless optical data injection by shining light onto a very small detector so that sufficient voltage swings are created directly on the chip to drive small digital blocks. Using the superior timing properties of short optical pulses as our source, we can apply the technique for *receiverless optical clock injection*. The technique can be very helpful in (de)multiplexing systems where accurate and precisely-controlled clocks are essential.

The design of optically triggered on-chip samplers is another application where we believe receiverless clock injection can be extremely useful. Indeed, the optical injection scheme not only defines a much better rising edge in the system, but it also allows on-chip samplers to be implemented without any high-speed connections attached to them, greatly simplifying their integration with normal circuitry.

Based on these first results, we can conclude that receiverless optical clock injection could be turned into a practical solution to optically trigger specialty time-critical sub-circuits on standard CMOS chips.

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