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Optical interconnect operation with high noise immunity

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Abstract: We demonstrate a modulator-based chip-to-chip link operation with an array of differential integrating receivers with a very low total optical power penalty of 0.12dB for 100mV of supply noise in receivers.

Parallel operation of large two dimensional optical I/Os can provide the throughput needed in electronic applications. These I/Os need to be placed close to digital circuits to minimize the latency. Simultaneous operation of this large array along with the operation of nearby digital circuits generates noise on the supply in the form of switching noise. The magnitude of this noise can be 100s of mV. Noise on the chip is also generated by carrier injection into the substrate. We demonstrate the operation of a link with high immunity to supply and substrate noise. A total link power penalty of only 0.12dB/100mV of receiver supply noise was observed. Link performance was unaffected by substrate noise injection from a voltage controlled oscillator (VCO). This high immunity can be attributed to the differential nature of the receiver. The effect of supply noise and crosstalk on electrically single-ended receivers has been studied [1] [2]. To the best of our knowledge, however, this is the first demonstration of the operation of an entire chip-to-chip optical link with modulators and electrically differential receivers quantifying the effect of supply and substrate noise.

A chip-to-chip optical link was operated as shown in figure 1. A silicon chip fabricated in a 0.5μm process contained a pseudo random bit sequence (PRBS) generator (2^{22} - 1) to drive the modulator array and a bit error rate tester (BERT) connected to the receivers. Hybrid integrated GaAs based modulators had a contrast ratio of 1.5 with 3.3V swing and the same devices acting as photodiodes had responsivity of 0.13A/W. The capacitance of these devices was 250fF, which limited the performance of the link.

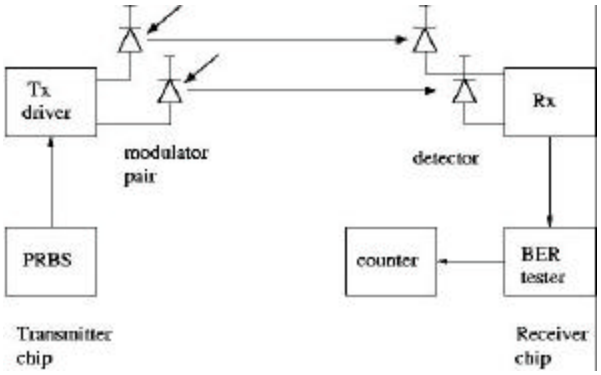

Fig.1: Schematic diagram of the chip-to-chip link operation with on-chip bit error rate tester

An integrating receiver based on positive feedback was used (figure 2). This receiver was tested with directly modulated lasers up to 600Mbps and the electrical power consumption of the receiver was only 2.3mW. The eye diagram of the operation is shown in figure 2.

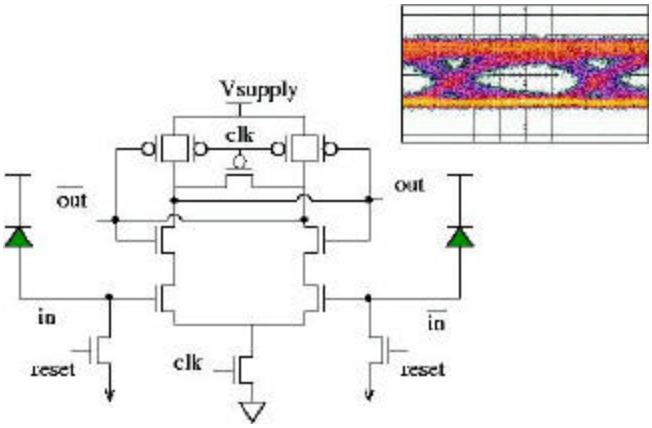

Fig.2: Circuit diagram of the integrating receiver. Eye diagram for 600 Mbps operation of the receiver is shown in inset

A square wave of different magnitudes and different frequencies was injected on the receiver supply to test the robustness of the link. Though the entire link operated at 400Mbps with very low bit error rate (below 10^{-9}), the noise measurements were done at 100 Mbps due to experimental limitations. As seen from the bit error rate plot in figure 3, the power penalty due to injected noise was only 0.12dB/100mV of supply noise at 1KHz. Bypass capacitors were connected to the receiver supply reducing the power penalty even further for supply noise above 100KHz. Electrical crosstalk from other receivers is accounted for in this measurement because they were toggling randomly. To observe the effect of substrate noise, a VCO was operated at different frequencies in the vicinity of the receiver. Receiver performance was unaffected by the VCO operation demonstrating that the substrate noise generated by the VCO did not create any power penalty. More results on receiver operation under optical crosstalk will be presented at the conference, but these results are very encouraging for use of dense arrays of optical interconnects in digital chips.

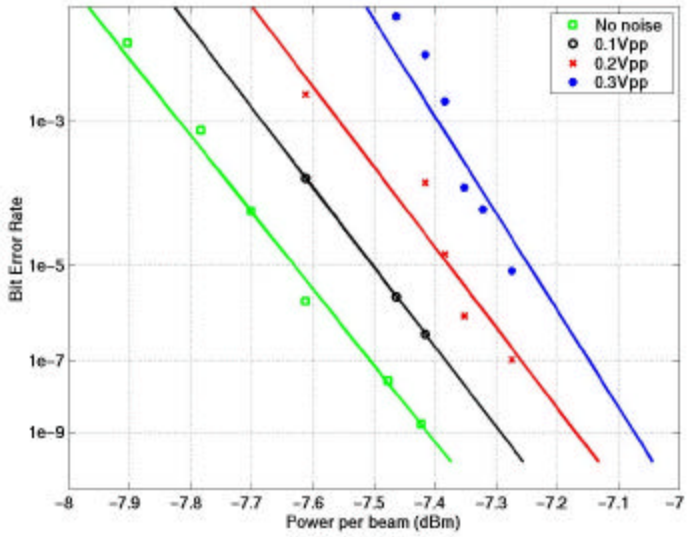

Fig 3: Bit error rate plots for entire link operation with supply noise injection to receivers

References

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