Novel On-Chip Fully Monolithic Integration of GaAs Devices With Completely Fabricated Si CMOS Circuits

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***Abstract*—We monolithically integrated polycrystalline GaAs metal-semiconductor-metal (MSM) photoconductive switches with a completely fabricated Si-CMOS amplifier and obtained a properly functional optical receiver, without altering the Si circuit performance. To our knowledge, this is the first time a fully monolithic on-chip integration has been achieved.**

***Index Terms*—Analog-to-digital converter (ADC), GaAs on Si, integrated optoelectronic CMOS circuit, metal-semiconductor-metal (MSM) switch, molecular beam epitaxy (MBE), monolithic integration, on-chip integration, optical receiver, photoconductive switch, polycrystalline GaAs (poly-GaAs).**

I. Introduction

WHILE Si-CMOS circuits with ever higher density and speed dominate most high-performance electronics, III–V semiconductor optoelectronics still dominate high-bandwidth regimes, such as telecommunications, optical communications and high-frequency instrumentation. As both technologies quickly advance, more applications could benefit from coupling Si-ICs with III–V optoelectronic components and high-speed circuits. As Si-ICs become ever more powerful and complex, fundamental limitations, such as signal skew, clock jitter, maximum clock frequency, high-speed I/O, pin count, and power dissipation are all identified as significant barriers to continued progress. Optical interconnects have been an attractive candidate to alleviate many of these problems and enable optical transmission of inter-and intra-chip signals. Despite recent progress in silicon optoelectronic devices, the technology is still far behind that of compound semiconductors in its ability to produce useful, integrated optical links. There are many applications where monolithic integration of compound semiconductor devices with Si could dramatically improve performance and functionality.

This paper describes monolithic integration of GaAs MSM detectors on completely fabricated Si CMOS circuits, which is an important alternate integration technique in our development of high-speed analog-to-digital conversion (ADC) systems [1] and [2].

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To overcome the bandwidth and aperture uncertainty limitations for all-electronic analog-to-digital converters, we investigated a time-interleaved, integrated photoconductive-sampling-based photonic A/D conversion system, utilizing low-temperature GaAs (LT-GaAs) metal-semiconductor-metal (MSM) photoconductive switches as optical sampling gates [1] and [2]. We previously combined high-speed LT-GaAs switches with a CMOS ADC chip using a flip-chip bonding hybrid integration technique and successfully demonstrated a high-bandwidth, two-channel prototype ADC system with less than 80 fs aperture uncertainty [1].

Monolithic integration is generally considered advantageous in order to minimize circuit parasitics. The commonly adopted approach for monolithic integration is to grow the GaAs (or other compound semiconductors) device layers onto the Si CMOS wafer prior to later level metallization and then finish the metallization after the growth of the GaAs devices. However, this approach creates significant fabrication complications due to the mismatch between the different equipment used for fabricating Si circuits and GaAs devices and potential cross-contamination issues. In prior work on monolithic integration of GaAs on Si, the final level of metallization was completed after growing the GaAs film at high temperatures. One severe problem in achieving the integration was the use of different lithography tools for GaAs and Si devices, and, hence, stitching differences between the two sets of tools made circuit yield suffer and the performance was seriously compromised [3]. Since our MSM switches with short switching aperture time are achieved by shortening carrier lifetime utilizing engineered material defects, we have explored the possibility of directly growing GaAs films at low temperatures on top of completely fabricated Si CMOS chips to enable on-chip, fully monolithic integration. With this simplified approach, all the problems described above are avoided.

The most critical issue in our approach is to prevent any modification of the characteristics of the underlying Si circuits from the GaAs film growth and processing steps. Novel low-k dielectric materials have been introduced and are becoming a routine for back-end-of-line (BEOL) applications in modern Si ICs. This creates severe limitations in the process temperature for subsequent deposition and treatment steps. This restriction is strongly influenced by the choice of the low-k films and different processing schemes. In general, a safe upper temperature limit is around 400 °C.

We initially studied the low-temperature epitaxial growth of GaAs (LT-GaAs) on Si [4] and [5]. MSM switches made from

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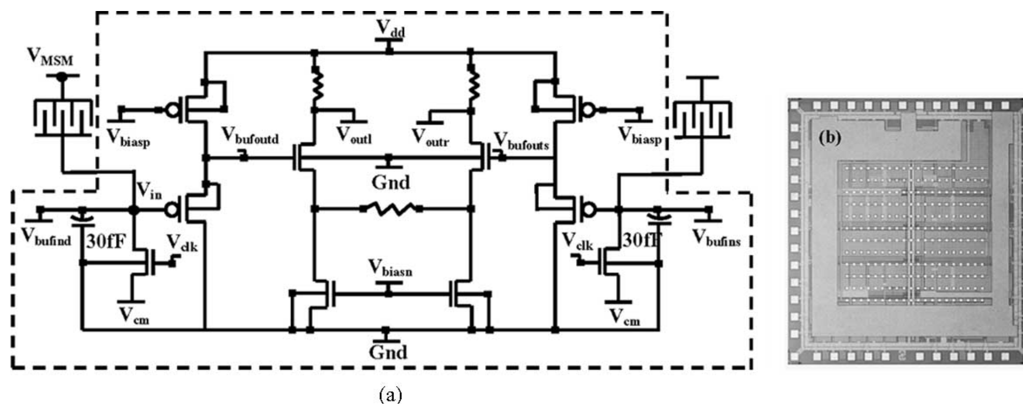

Fig. 1. (a) Circuit schematic of the CMOS receiver chip (inside the dotted line). The differential pair of the polycrystalline GaAs MSM switches is integrated at the receiver input nodes. (b) Completely fabricated CMOS receiver chip, before integration. Size is ~2 mm × 2 mm.

LT-GaAs on Si showed ~2 ps switching time and the responsivity was comparable to its counterpart on a GaAs substrate. However, modern ICs usually have six or more metal layers. In order to grow GaAs on the Si surface of a complete chip, deep etching through these interconnect layers is required to expose the Si surface. This creates deep trenches and causes metal step coverage problems. To keep away from this problem and simplify the processing, we boldly studied direct growth of GaAs on SiO_2 or Si_3N_4 at low temperatures. At around 400 °C, growing GaAs on amorphous dielectrics results in polycrystalline GaAs. The grain boundaries act as trapping and recombination centers, resulting in short carrier life time, which has a similar effect to the point defects in LT-GaAs that we previously used to achieve high-speed switching [4] and [5].

Using 1-μm-thick poly-GaAs films grown on SiO_2 at 400 °C, we made MSM switches with 1-μm finger width and 0.8-μm finger spacing. A full-width-at-half-maximal (FWHM) switching window of ~1.65 ps was obtained using an electro-optic sampling technique [4] under illumination of a 12.4 pJ (100 μW) Ti/sapphire mode-locked laser short pulse and with 1 V DC bias voltage. A Fourier transform of the measured pulse response indicated a ~270-GHz 3-dB bandwidth. The responsivity was as high as 80 mA/W under the above testing conditions.

II. Experiments and Results

A. Completely Fabricated Si Amplifier IC Chip

At the time of this study, a suitable high-speed ADC CMOS chip was not available to demonstrate our on-chip integration for ultrahigh-speed ADC system [1] and [4]. For a proof-of-concept, we used a moderate-speed (300 MHz) optical receiver Si IC chip that was available. As long as we can achieve a fully functional integrated system without degrading the Si circuit performance, this is sufficient to prove the validity of this integration approach.

Fig. 1(a) shows the circuit schematic of the receiver chip. It is a two-stage amplifier with a buffered input stage and a differential gain stage. The MSM switches are to be integrated at the input nodes. Fig. 1(b) shows the original completely fabricated CMOS chip before integration. The receiver was fabricated on an 8″ wafer and diced into a die approximately 2 mm × 2 mm in size. It has six layers of metallization and is passivated with SiO_2/Si_3N_4 dielectrics. The top metal layer is Al+0.5% Cu. The white squares in the picture are arrays of approximately 20-μm-square and 2-μm-deep glass cuts, which were originally made for flip-chip bonding purpose. The white color we see in the picture is the color of the final metal layer. Using this chip, we would like to grow poly-GaAs film on top, make the MSM switches on GaAs, and then connect MSM switches to the underlying Si circuits through the glass cut areas.

B. Chip Cleaning and GaAs Film Growth

Surface cleanliness is crucial for GaAs epitaxial growth during GaAs/Si monolithic integration. Typically, the cleaning of the Si surface is done at temperatures higher than 600 °C [4], which is not acceptable for a finished chip. Since we are targeting high-speed applications and controllable defects are welcome in shortening the carrier lifetime, the requirement is relaxed to some extent.

In our particular situation, the fact that the chip is already diced into small pieces created a considerable level of unnecessary complexity for GaAs film growth and integration processing, purely due to handling difficulties. In order to grow GaAs films on such small chips, we first had to mount the chip onto a 3″ carrier Si wafer. This was done by placing the chip on a hot plate in the cleanroom and applying a minimal amount of MBE-grade (molecular beam epitaxy) In on the back of the chip to adhere the chip onto the clean Si carrier wafer. Due to the small size of the chip and the large surface tension of In, attention must be given to avoid In migrating onto the top surface and the edge of the Si chip. If the integration was done for a full wafer, the extra effort in handling and processing due to the small size would not be required.

Chips were carefully cleaned by using multiple solvents: PRS1000, Shipley Microposit Remover 1165, PRX-127, acetone, methanol and isopropyl alcohol. PRS1000 is an organic solution used as a resist strip, where PRS stands for Positive Resist Stripper. It is used as a metal clean to remove organics and gross surface contaminants on metalized wafers. PRX-127 cleans strip resist but does not attack metals, provided it is anhydrous. The chip (on the carrier wafer) was loaded into the loadlock chamber of an MBE system and baked at 250 °C for

30 min to remove moisture and gases before it was moved to the transfer tube.

GaAs films were grown in a solid source Varian Gen II MBE system. Gallium flux was supplied by a thermal effusion cell and dimeric arsenic (As_2) was provided through a valved thermal cracker. A $\sim$1-μm-thick layer of undoped GaAs was grown at 400 °C substrate temperature (thermal couple reading) with an As_2/Ga beam-equivalent-pressure (BEP) ratio of 6. GaAs growth was initiated with ten migration-enhanced epitaxy (MEE) cycles and the wafer rotated at 10 r/min throughout the growth. Growing GaAs on dielectric layers and at this low temperature rendered the film polycrystalline. Because MBE growth is not selective, the poly-GaAs film covers the entire chip surface, including the glass cut areas.

C. Integration Process

If not considering the needless difficulties caused by the very small size of the chip, the process is quite simple, which is exactly the beauty of this approach.

Fig. 2 illustrates the detailed steps of the integration process. The highest temperature step was the poly-GaAs film growth in MBE chamber (400 °C), which is safe for all modern IC fabrication processes, including circuits using Al interconnect and low-k dielectric materials.

Step 0 shows the starting chip, with dielectrics passivating the surface, and arrays of glass cuts made to expose the top metal layer for later contact.

In the first step, the chip is cleaned using the method described above and then loaded into MBE chamber. A 1-μm-thick poly-GaAs film was then grown at 400 °C over the entire chip surface, including the glass cuts.

Next, the MSM photoconductive switches were patterned on the top poly-GaAs film. Eight switches (four differential pairs) with an interdigitated pattern were fabricated by depositing titanium/gold contact metal on the poly-GaAs layer through a standard lift-off process. E-beam lithography was used to fabricate switches with 0.8 μ and 0.6-μm finger spacing and $\sim 15 - \mu$m finger width.

In order to connect GaAs switches with Si circuits, the poly-GaAs grown inside the glass cut area had to be removed in order to expose the top metal layer of the Si chip. With photoresist protecting the switch areas, the unwanted poly-GaAs was wet etched in citric acid, which is highly selective between GaAs and Al.

The final metal contact is applied using three-step deposition, a vertical deposition followed by two angled evaporation steps from both sides to ensure good step coverage because there were many steps on the surface at this point. We first deposited 150 Å Cr + 850 Å Cu + 500 Å Au vertically. Au is the dominant metallization on GaAs circuits. Cr and Cu were used to avoid the Au_2Al "purple plaque" intermetallic compounds [6]. Then, in the first oblique deposition, 200 Å Cr + 1000 Å Au were evaporated at a 60° angle from one side. This is followed by a second evaporation of the same thickness layers at the same angle, but from the opposite direction. This kind of deposition ensured conformal coverage of the contact metal.

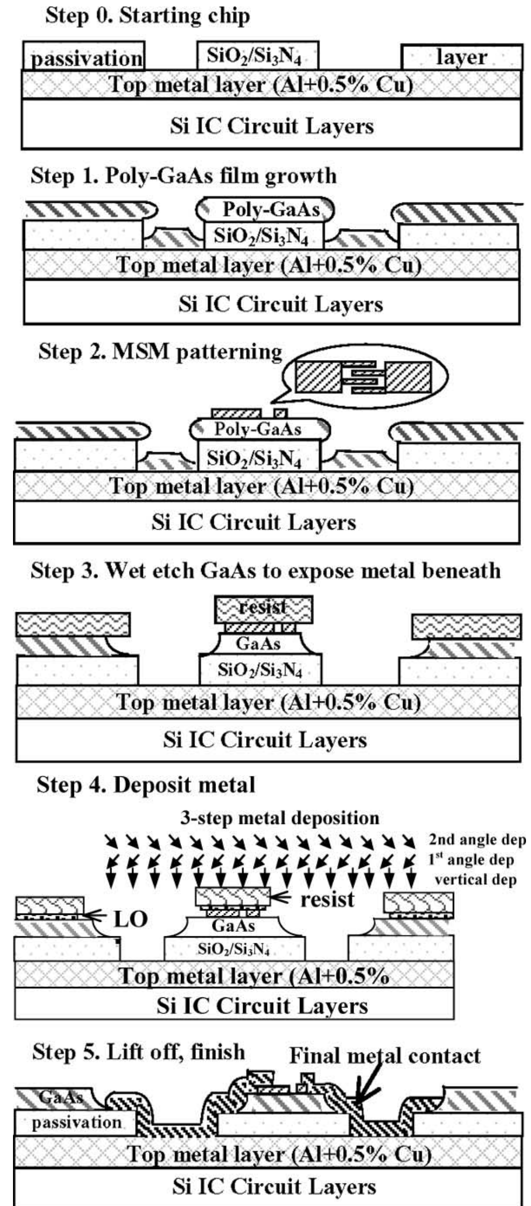

Fig. 2. Monolithic integration process to fabricate GaAs MSM switches directly onto completely finished Si amplifier chip and to achieve an integrated optical receiver system. Not drawn to scale. Each step has self-explanatory subtitles.

Metal deposition from different angles potentially makes the lift-off process very difficult, if not impossible. We used a LOL2000 dual layer resist lift-off process to bypass the possible non-lifting problem. LOL2000 is a non-UV-sensitive liquid polymer, which can be etched away with most standard developers (weak bases). LOL2000 was first spun on the wafer and baked. Then, standard photoresist was spun on and soft-baked. The photoresist was exposed and developed in the normal manner. During development, the standard developer cleared the exposed photoresist, and also etched away some LOL2000, depending on how long it was in contact with the developer. This leads to undercutting of the photoresist and this overhang prevents LOL sidewall deposition of metal films in the angled evaporation and created an air gap for lift-off. The resist was

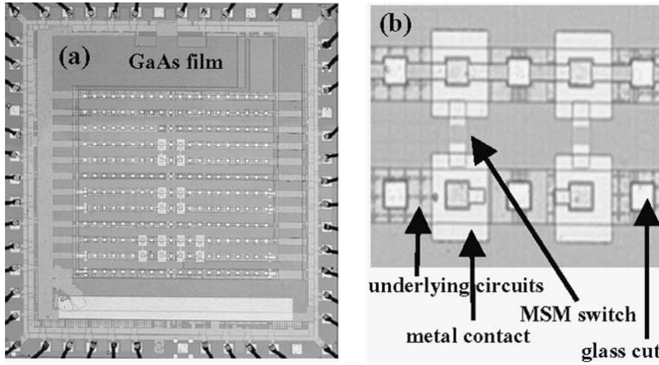

Fig. 3. (a) Optical receiver after integration. The gray areas are poly-GaAs film and the eight golden devices are MSM switches. (b) Enlargement of a pair of MSM switches. The large square metal pads connect the MSM switches to the underlying Si amplifier circuit.

lifted-off using Microposit 1165 and acetone. Because the overhang profile is caused by undercutting the resist, care must be taken to avoid completely undercutting (and therefore lifting off) narrow geometries [7].

After lift-off, the integration was complete. MSM switches were connected to the Si circuits through the glass cut areas and an integrated optical receiver system was obtained.

D. Monolithically Integrated Optical Receiver

Fig. 3(a) shows a micrograph of the fully integrated optical receiver. The dark gray areas are where GaAs was grown. Four pairs of differential poly-GaAs switches are shown in Fig. 3(a).

Fig. 3(b) is a zoomed-in picture showing the details of one such pair. The large rectangular metal pads connect the MSM switches with the underlying Si amplifier circuit.

E. Optical Receiver Testing

We characterized the MSM switches made from 1-μm-thick poly-GaAs grown on SiO_2 under the same conditions and achieved fast switching speed with high responsivity. We reported the executive summary results of the switches in the introduction session of this article. Fig. 4 shows the temporal and frequency response of one such switch. Since this receiver chip was not designed for high-speed applications, we were unable to directly characterize the high-speed switch performance for the integrated system. Instead, to prove the soundness of our monolithic integration approach, we tested the dc characteristics of the integrated receiver with the MSM switches to verify if it was functional as designed.

Fig. 5 shows the dc characteristics of the optical receiver. With a constant continuous-wave (CW) laser power triggering the switch, the MSM bias voltage (V_{MSM}) was varied to indirectly change the input node voltage (V_{in}) of the receiver (see Fig. 1). The corresponding output voltage (V_{out}) was recorded to obtain the dc transfer function. Changing the laser power, a different photocurrent (and therefore another transfer function) was generated. In this experiment, we indirectly measured the transfer function of the integrated receiver and demonstrated that after integration, we achieved a properly functioning optical receiver with typical input–output characteristics.

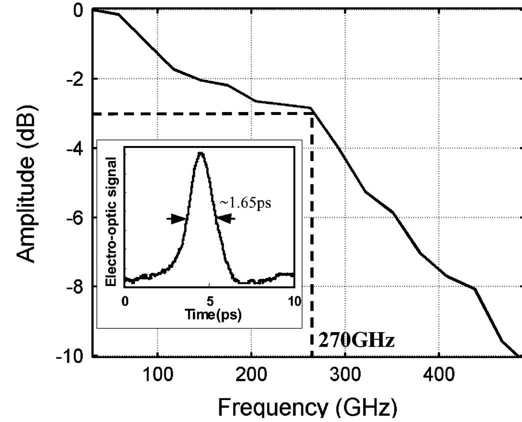

Fig. 4. Frequency response of a poly-GaAs MSM switch. Poly-GaAs was grown at $\sim 400\,^{\circ}$C. The inset is the temporal response measured by electro-optic sampling. The FWHM is ~ 1.65 ps. The 3-dB bandwidth of this switch is 270 GHz by performing Fourier transform on the waveform. The MSM switch has a 1-μm finger width and a 0.8-μm finger spacing. The response shown was tested under 1 V bias voltage and 12.4 pJ pulse energy, using electro-optic sampling technique. Responsivity was 80 mA/W for this switch.

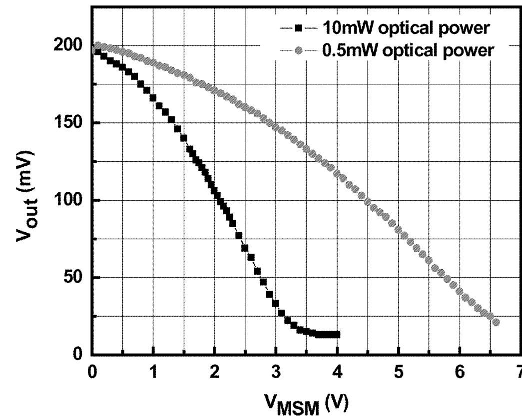

Fig. 5. Input-output characteristics of the integrated optical receiver with MSM switches. CW laser $\lambda = 850$ nm.

It is very important that the integration process not affect the Si circuit performance. We fed the amplifier with two differential electrical signals, and used a sampling oscilloscope to measure the output step response in order to compare the AC characteristics of the amplifier (without MSM switches) before and after the integration. Fig. 6 confirms that the change in step response is not detected. The rise times of the amplifier before and after integration are both ~ 11 ns. The difference is ~ 0.1–0.2 ns. The measurements were done on two different chips of necessity. One was as-fabricated and did not go through the integration process, while the second was used in our integration. Because it is necessary to wire-bond the chip to the testing board in order to perform the electrical testing, it is impossible to characterize the same chip before and after integration. In addition, during the course of our work, Si chips that we received from different wafers (even possibly from different wafer lots) had chip-to-chip variations of ~ 0.2 ns, very similar to what we measured in the before-and-after integration chips and all were fully functional. The amplifier gain is measured to be 3 for chips before and after

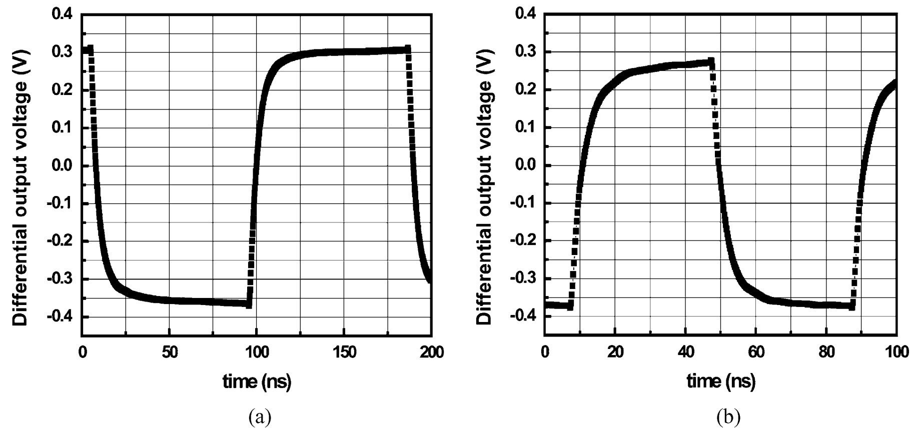

Fig. 6. Step response of the amplifier (a) before and (b) after integration. The 10–90% rise time in (a) and (b) are both ~11 ns and the difference is ~0.1–0.2 ns. The amplifier gain is both 3. Circuit biasing conditions are: $V_{\rm dd} = 2.5$ V; $\rm Vclk = 0.66$ V; $\rm Vcm = 0$ V; Vbias,$n = 0.79$V; Vbias,$p = 1.9$ V.

integration. Additionally, the circuit biasing points stay exactly the same. These results clearly prove that our approach is completely safe for a finished Si CMOS chip with metallization. The circuits are fully functional and within experimental error, unchanged.

III. Summary

We have monolithically integrated polycrystalline GaAs MSM switches with a completely fabricated CMOS amplifier IC chip and obtained a properly functional optical receiver without modifying the underlying Si circuit performance. The GaAs film growth, integration process, and the electrical and optical testing of the integrated system have been described in detail. The beauty of this integration approach is its simplicity, minimum fabrication disturbance, limited entirely to the tail-end Si processing, and greater applicability for much broader areas, such as optoelectronic interconnects for very-high-density, very-high-speed CMOS circuits.

In addition to minimizing parasitics (in contrast to hybrid integration methods such as flip-chip bonding), the monolithic integration avoids the use of bulk GaAs, and therefore substrate removal [8]. High-cost GaAs material is saved, and it is much easier for mass-production.

For suitable niche applications, our approach can achieve very large scale compact integration, with much better alignment with Si circuits. Another benefit is that, for optoelectronic systems, by covering the chip surface with a layer of GaAs, the potential for scattered light affecting the CMOS circuit is greatly reduced.

Previous studies reported integration of GaAs devices with partially fabricated Si circuits. To our knowledge, this is the first time a fully monolithic on-chip integration has been successfully achieved.

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