1550nm Optical Interconnect Transceiver with Low Voltage Electroabsorption Modulators Flip-Chip Bonded to 90nm CMOS

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Abstract: A low-voltage 90nm CMOS optical interconnect transceiver operating at 1550nm is presented. This is the first system demonstrated using the recent Quasi-Waveguide Angled Facet Electroabsorption Modulator (QWAFEM), featuring simple electronic and optical packaging.

OCIS codes: (060.4510) Optical communications; (230.4110) Modulators

1. Introduction

We demonstrated an optical interconnect transceiver operating at 1550nm utilizing the recent QWAFEM architecture [1]. These modulators combine benefits of waveguide modulators and surface-normal modulators. Advantages for packaging these devices include simple integration with CMOS via flip-chip bonding, arrayability in two dimensions, displaced surface-normal optical input and output ports, and misalignment-tolerant optical coupling. They also obtain useful contrast at a low (2V) drive voltage and operation has previously been demonstrated over a wavelength range of 16nm. The transceiver is fabricated in a 90nm CMOS process and employs a novel pulsed-cascode driver [2], capable of supplying an output voltage swing of 2V (twice the nominal 1V CMOS supply) without overstressing thin-oxide core CMOS devices. The transceiver achieves 1.8Gb/s operation with a power consumption of 23.6mW. To the best of our knowledge this is the first demonstration of an interconnect transceiver operating at 1550nm with a III-V output device directly integrated to CMOS.

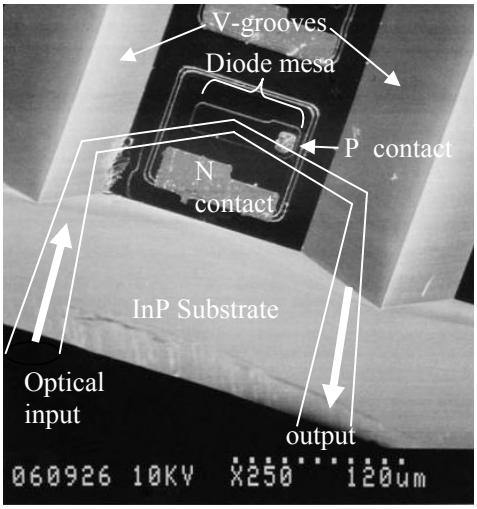

Fig. 1. SEM image of QWFAEM modulator with overlaid optical path and annotation

2. Modulators and Transceiver Circuit

The modulators used are shown in Fig. 1. They are fabricated on a double-side polished (100) InP wafer with epitaxially grown InGaAsP/InP layers comprising a PIN diode containing a multiple quantum well (MQW) structure in the intrinsic region. The active region is surrounded by two selectively etched mirrors. The input and output beams pass through the substrate, and the optical path has three internal reflections, two from the selectively etched mirrors and one reflection from the interface between the epitaxially grown InGaAsP and air. The grazing incidence

increases the interaction length with absorbing material, and a resonant cavity is formed between a distributed Bragg reflector in the N-doped epitaxy and the epitaxy-air interface, further enhancing absorption. Unlike in a waveguide modulator where propagation along the absorbing material is accomplished by coupling to a waveguide mode, there is no modal constraint imposed in coupling through the active region at grazing incidence, easing optical alignment. Furthermore, the triple-bounce geometry results in a fixed separation between input and output beams for small translations of the input beam across the modulator substrate surface. As a result, it should be possible to perform a one-step alignment of an entire array of lensed fibers for input and output coupling to the modulator chip, provided the pitches of the fibers and the modulators are matched.

Building upon previous work [1], in this implementation of the QWAFEM, the spacing of modulators was changed to match the pitch of the CMOS transceiver chip, and diode mesas were resized to reduce capacitance. Several varied epitaxial wafers were grown and tested to achieve a precisely tuned resonant cavity despite run-to-run variability in the epitaxial growth.

Fig. 2 shows the optical interconnect transceiver architecture implemented in a 1V 90nm CMOS technology. In order to enable short bit periods without consuming excessive area and power in clock generation and distribution, a multiple clock phase multiplexing architecture is used at both the transmitter and receiver. In the transmitter frequency synthesis PLL, a five-stage ring oscillator provides five sets of complementary clock phases spaced a bit period apart. These phases are used to switch a multiplexer to produce a serial data stream with a data rate of five times the clock frequency. The multiplexer serial output is then buffered by the modulator driver output stage [2]. At the receiver side, an integrating and double-sampling front-end [3], performs demultiplexing directly at the input node using five uniform clock phases from the clock recovery system.

The modulator driver uses a pulsed-cascode output stage in order to supply an output voltage swing of 2V (twice the nominal 1V CMOS supply) to the QWAFEM. Pulsing the gates of the cascode transistors during transitions allows this driver to eliminate the drain-source voltage (V_{ds}) overstress present in static-biased cascode drivers [4], and prevents transistor degradation from hot-carrier injection [5].

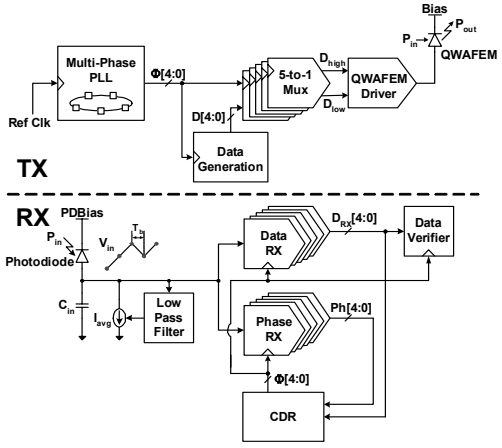

Fig. 2. Optical transceiver architecture

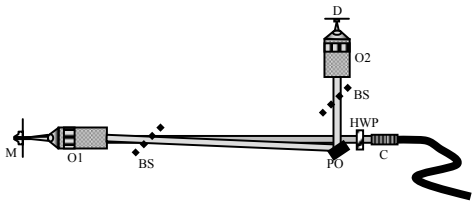

Fig. 3. Transceiver link schematic. Linear-polarized light enters through the fiber and free-space collimator (C), and rotatable half-wave plate (HWP). Focusing onto the QWAFEM modulator (M) is accomplished by a microscope objective (O1), and the spatially displaced output beam of the modulator is reflected by the pick-off mirror (POM) into a second microscope objective (O2) and onto a detector (D). Alignment of the beam on the modulator and detector is accomplished an IR camera (not shown) and illumination and with two removable pellicle beamsplitters (BS).

3. Experiment

An array of InP QWAFEMs was flip chip bonded to the CMOS transceiver chip with eight transmit channels. The chip is placed in an open-cavity surface-mount package on a test board mounted on a 3-axis translation stage. An HP8133A pulse generator supplies the reference clock to the transmitter PLLs and the transmit data sequence is controlled with an on-chip 20-bit register that can be programmed with a computer via a serial testing interface.

The optical link is shown in Fig. 3. 1550nm light is coupled from single mode fiber into a free space collimator. The collimator was followed by a half-wave plate, facilitating alignment such that the linear polarized light in the resonator would be TE polarized for optimal performance. A microscope objective focused the collimated beam to a 12um diameter spot. The focused beam is coupled into a QWAFEM. Between the collimator and objective, a removable pellicle beamsplitter was used for alignment of the beam with the modulator array. The entry and exit points on the array's substrate are displaced by 200 μm. After collimation by the microscope objective, the beam exiting the modulator is separated for detection by a pick-off mirror, and focused onto a 20μm diameter 20GHz

photodetector. The photodetector is attached to a receiver on a second identical CMOS transceiver chip via short wire-bonds. This chip is also packaged and attached to a test board mounted to a 3-axis translation stage. The received data is verified with an on-chip 20-bit register whose output can either be scanned-out to a computer or observed on an oscilloscope.

4. Results of high speed testing

While the CMOS transceiver was designed to nominally operate at 5-16Gb/s, the rise time of QWAFEMs did not permit operation at that speed. When the chip was triggered too slowly its performance degraded due to limited voltage-controlled oscillator (VCO) range. Thus, in order to get meaningful results from the transceiver link, we synthesized a repeating 10-bit pattern by specifying the 20-bit sequence in pairs of bits to allow the VCO to operate at a higher frequency. Since the receiver chooses the decision threshold based on the average current at the photodetector, it was necessary to send signals with an equal number of ones and zeros. We tested several bit patterns, attempting to generate the worst-case detection scenario available with 10 bits. By taking a histogram of each of the worst-case bits in the pattern we were able to estimate the error rate. Transmission of 10-bit sequences was tested over a range of 1Gb/s to 1.8Gb/s. At 1.8Gb/s with an average detected power of -15.2dBm, the BER estimated from the histogram was 10^{-10}. The bit timing margin was such that the BER was estimated at less than 10^{-9} over a total range of phase shift of the receiver clock of 47% of the period of one bit.

The total transceiver power dissipation is 23.6mW at 1.8Gb/s. The transmitter power makes up 15.2mW, with 3.8mW to drive the QWAFEM, 8.8mW for the multiplexer and buffers, and 2.6mW for the TX PLL. The receiver consumes 8.4mW, with 4.5mW from the integrating/double-sampling front-end, and 3.9mW from the clock recovery circuitry.

5. Conclusions

We demonstrated an optoelectronic interconnect transceiver at 1550 nm. This is to our knowledge is the first demonstration of an interconnect at that wavelength using a output device directly bonded to CMOS. The modulators used are practical for integration with CMOS due to their low drive voltage of 2V and their lack of need for external high-speed packaging. They are practical for optical systems because of their surface normal input and output ports, two-dimensional arrayability, tolerance to beam misalignment, and broad bandwidth of operation. The transceiver achieves 1.8Gb/s operation with a low total power consumption of only 23.6mW.

6. References

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