Selective-Area Growth of Ge and Ge/SiGe Quantum Wells in 3 μm Silicon-on-Insulator Waveguides

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Abstract: We demonstrate a robust process for growing high-quality bulk Ge and Ge/SiGe quantum wells in selected areas of 3 μm thick silicon-on-insulator waveguides, eliminating sidewall growth and hence facilitating low-insertion-loss optical modulators.
OCIS codes: (160.2100) Electro-optical materials; (230.4205) Multiple quantum well (MQW) modulators.

1. Introduction and motivation

Ge and especially Ge/SiGe quantum wells exhibit strong electroabsorption (Franz-Keldysh effects and the quantum confined Stark effect (QCSE), respectively), which make possible the development of Si-compatible optical modulators for optical interconnect applications [1]. Waveguide-based modulators allow for longer interaction lengths between the optical beam and the active material and easier integration with other on-chip optical components. However, to minimize loss from background absorption in Ge structures, the modulator region must be integrated with other low-loss entrance and exit waveguides, such as silicon-on-insulator (SOI) waveguides. Here, we develop a reliable substrate preparation process that enables this selective-area growth (SAG) and demonstrate high-quality selective-area growth of Ge and Ge/SiGe quantum wells.

2. Selective-area growth substrate requirements

When growing directly into a hole cut into an SOI waveguide, due to the long diffusion length of the Ge and Si atoms in the reduced-pressure chemical vapor deposition (RPCVD) system used for the epitaxial growth, SiGe growth is initiated on the exposed Si crystalline sidewall as well as the desired region at the bottom of the growth window. As shown in Fig. 1, this leads to undesired sidewall growth as well as poor quality growth within the growth windows. The sidewall growth is detrimental because it can lead to shorting of the *p-i-n* diode region which contains the QWs in the intrinsic region. It can also significantly disturb the planar heterostructure of the device.

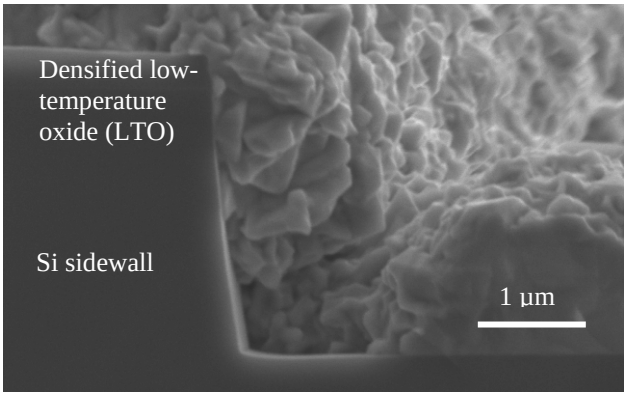

Fig. 1 Cross-section scanning electron microscope (SEM) image of selective-area growth window without any dielectric spacer. Poor quality growth is present both on the Si sidewalls and the bottom of the growth window.

Selective-area epitaxial growth of Ge/SiGe QWs directly on a bulk Si substrate with thermal SiO_2 serving as a growth mask has been demonstrated [2] in our group, allowing the first, proof-of-principle Ge QW waveguide modulators [3]. This epitaxial growth showed high-quality crystal growth inside the growth windows and crystal faceting at the edges of the growth windows, with no growth on the oxide sidewalls. To obtain low-insertion-loss devices, however, we need a robust process capable of mode-matched integration with standard SOI waveguides, which means the growth windows must be etched partially through both the top oxide growth mask layer and the Si device layer of the SOI waveguides, enabling optimal mode overlap of the optical mode and the absorbing QWs.

To prevent sidewall growth and enable high-quality growth in the desired regions, a process was previously proposed to deposit a dielectric spacer on the sidewalls of the growth windows [4]. Fig. 2a shows a schematic of the designed substrate, with QW growth in the growth window. Unfortunately, while this spacer fabrication process did allow the demonstration of high-quality QW growth, it was not robust to minor fabrication variations, making mode-matched growth in the 3 µm guides unreliable. Fig. 2b presents a typical result, with excessive sidewall growth visible and planar QW growth at the center of the growth window.

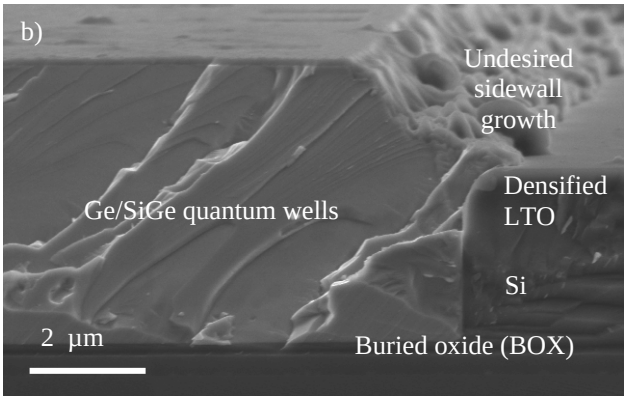

Fig. 2 a) Schematic of desired growth substrate with dielectric spacer on growth window walls. b) Results of previously proposed spacer fabrication process, with Ge/SiGe QWs and visible sidewall growth.

To overcome this problem, we propose a change in the spacer fabrication process set forth in [4] that renders it independent of process variations. Follow the dry etch of the growth window, the Si sidewalls are etched in room temperature tetramethylammonium hydroxide (TMAH) to undercut the Si sidewalls. Then, the wafer is oxidized, to form the spacer layer. Finally, a dry etch and very short wet etch in 20:1 buffered oxide etch (BOE) are used to remove the oxide from the bottom of the growth window while leaving it on the sidewalls. The key to the success of this process is the presence of the overhanging densified LTO growth mask, which serves to protect the spacer on the sidewalls from being etched during the dry etch. Fig. 3a illustrates the target design for the growth substrate.

3. Results and conclusion

As shown in Fig. 3b, this altered design reliably leads to high-quality Ge growth with minimal sidewall growth. Furthermore, the crystal faceting at the sidewalls that was first shown in selective-area growth of Ge/SiGe QWs on bulk Si is evident, showing well-controlled growth. This process is also simpler than the previous version, with fewer process steps. This development and demonstration of a robust process for preparing substrates for selective-area epitaxial growth should enable future integrated low-loss high-performance Ge/SiGe QW waveguide modulators monolithically integrated with SOI waveguides.

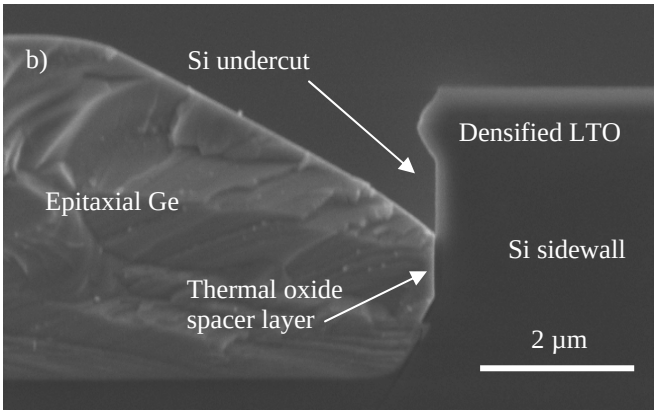

Fig. 3a) Schematic of new spacer fabrication, with Si undercut and overhanging densified LTO growth mask which protects the thermal oxide spacer on the growth window sidewalls. B) Cross section SEM of Ge growth on a TMAH-etched substrate with oxide spacer protecting the sidewalls. Crystal facet at sidewall is evidence of successful spacer fabrication.

4. References

[1] Y. H. Kuo, Y. K. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller and J. S. Harris, Strong quantum-confined Stark effect in germanium quantum-well structures on silicon," Nature 437, 1334-1336 (2005).
[2] R. Shen, Y. Rong, T. I. Kamins, J. S. Harris, and D. A. B. Miller, "Selective epitaxial growth of Ge/Si0.15Ge0.85 quantum wells on Si substrate using reduced pressure chemical vapor deposition," Appl. Phys. Lett. 98, 151108 (2011).
[3] S. Ren, Y. Rong, S. Claussen, R. Schaevitz, T. I. Kamins, J. S. Harris, and D. A. B. Miller, "A Ge/SiGe Quantum Well Waveguide Modulator Monolithically Integrated with SOI Waveguides," 8th Int. Conf. Group IV Photonics, London, Sept. 2011, Paper WA3
[4] S. Ren, T. I. Kamins, and D. A. B. Miller, "Thin Dielectric Spacer for the Monolithic Integration of Bulk Germanium or Germanium Quantum Wells With Silicon-on-Insulator Waveguides," IEEE Photonics Journal, 3, 739-747 (2011).