Novel Si-based Optoelectronic Switching Device: Light to Latch

Ali K. Okyay, Abhijit J. Pethe, Duygu Kuzum, Salman Latif, David A. B. Miller and Krishna C. Saraswat

Department of Electrical Engineering, Stanford University, Stanford, CA 94305, U.S.A.

420 Via Palou, CIS #13, Stanford, CA 94305-4070, Ph (650) 725-3612, Fax (650) 725-6278, email:aokyay@stanford.edu

Abstract: A novel, high performance optoelectronic switch is introduced. The device is a Si-MOSFET with Ge gate that can be fabricated at the nanoscale with very low capacitance. Current gain of up to 1000× is demonstrated.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (250.5300) Photonic integrated circuits

Increasingly more research focuses on chip-to-chip and on-chip optical interconnects as an alternative to address the power dissipation, delay and bandwidth problems faced by copper wires [1]. Compound semiconductors have been the forerunner in optoelectronic applications, but their integration with Si is expensive and problematic. Recently, it has been demonstrated that incorporation of Ge into Si is promising to design low-cost modulators on Si with potentially higher efficiencies than their hybrid counterparts [2]. This technology is fast approaching to replace the conventional building blocks of the transmitter end in an optical link operating at telecommunication standard wavelengths. Si-based classical optical receivers suffer from large photodiode capacitance hence dissipate huge amounts of power besides occupying a large footprint. Increasingly stringent power requirements on a chip limit the total number of receivers, hence the number of links.

We propose a complete reform in the design of the receiving end of an optical link by replacing a classical receiver with an optoelectronic switching device. By such a design, light can be introduced at the latch level eliminating the ever so power-hungry electrical interconnection hierarchy of clock distribution networks as well as the high capacitance optical detectors [3]. The device scales with technology and can be made extremely compact for very low capacitance and small footprint area.

The proposed device is a MOSFET with a Ge gate and the rest of the device is in Si, as depicted in Fig. 1. Signal is generated remotely and is transmitted as optical energy in the 1330-1550nm window where Ge is a strong absorber. Optically generated carriers move within the gate due to band bending and the applied gate bias, as shown in Fig. 2. This constitutes a gate current which in turn modifies the channel electrostatics, inducing a highly amplified drain current. Si, however, is transparent at these wavelengths, so no absorption takes place in the channel; hence the surrounding Si circuitry is noise free, providing noise immunity from signaling. As light is turned off, the gate oxide capacitance discharges through both increased recombination in the gate depletion region and diffusion due to gradient in the carrier concentration. The speed of the device is limited by turn-off which can be controlled by carrier lifetimes and thickness of the polycrystalline gate region.

2-D electrostatic and transient device simulations were done using MEDICI^{TM}. The Ge-SiO_2-Si capacitor governs the operation of the device. Fig. 3(a) plots capacitance of the stack versus voltage curves for varying light intensity. The capacitance is modified by light because the optically generated carriers in the gate depletion region act as an extra source of charge. Due to capacitance change, $Q_{inversion}$ is also modulated with incoming light. To verify simulation results, we fabricated Ge-SiO_2-Si structures by depositing Ge on thermally grown SiO_2. Fig. 3(b) plots the measurement results showing capacitance changing with light as predicted by simulations.

Si NMOS transistors with 250nm polycrystalline Ge gate deposited on 6nm thermally grown SiO_2 were fabricated. An internally modulated 1.55μm laser with a synchronized lock-in amplifier was used to precisely extract the photocurrent component of the measured signal. Fig. 4 plots the measured optical gate and drain currents versus the gate voltage for V_{GATE}=V_{DRAIN}. The observed drain current is up to 3 orders of magnitude larger than gate current, which can be attributed to the amplification of the transistor.

Unlike classical optical receivers, complementary operation is also attainable in this device scheme by simply tailoring the doping in the gate and channel regions. An enhancement mode device turns on with light and a depletion mode device, however, is normally on, and turns off when illuminated with light. These devices can be connected as a CMOS inverter to fashion an optoelectronic latch with light as the input signal. Transient response of such a device plotted in Fig. 5 shows that the device can drive the next stage, minimum sized inverter, rail-to-rail with no additional amplification. The device can easily achieve 10Gbps operation and is promising to operate in excess of 20Gbps with further optimizations.

This optoelectronic switch can be fabricated at the nanoscale along with deeply scaled conventional MOSFETs using advanced Si technology. Such a device has extremely small capacitance and hence can potentially be very fast. The intrinsic speed of the device can be improved by tailoring the built-in band bending using a graded SiGe gate region. Plasmonic coupling could be used to focus light on such nano-scale dimensions by nano-metallic structures to further enhance device performance [4].

References

[1] D. A. B. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," Proc. IEEE **88**, pp. 728-749 (2000).

[2] Yu-Hsuan Kuo, Yongkyu Lee, Yangsi Ge, Shen Ren, Jonathan E. Roth, Theodore I. Kamins, David A. B. Miller & James S. Harris, "Strong quantum-confined Stark effect in germanium quantum-well structures on silicon," Nature **437**, 1334-1336 (2005).

[3] H. Cho, P. Kapur, and K. C. Saraswat, "Power Comparison Between High-Speed Electrical and Optical Interconnects for Interchip Communication," J. Lightwave Technol. **22**, 2021-2033 (2004).
[4] L. Tang, A. K. Okyay, J. A. Matteo, Y. Yuen, K. C. Saraswat, L. Hesselink, D. A. B. Miller, "C-shaped Nano-Aperture-Enhanced Germanium Photodetector," Opt. Lett., **31**, 10, 1519-1521 (2006).

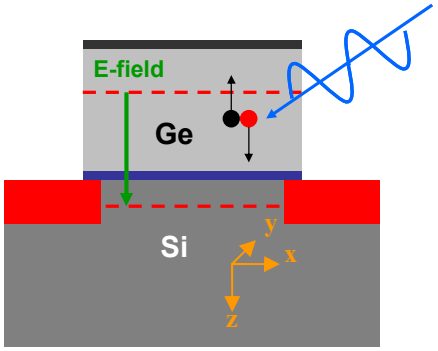


Fig. 1: Schematic of the optoelectronic switch. Source/drain and channel regions formed in Si. Ge gate is deposited on thermally grown SiO_2. Absorption takes place in the gate. Si is transparent and hence is noise immune.

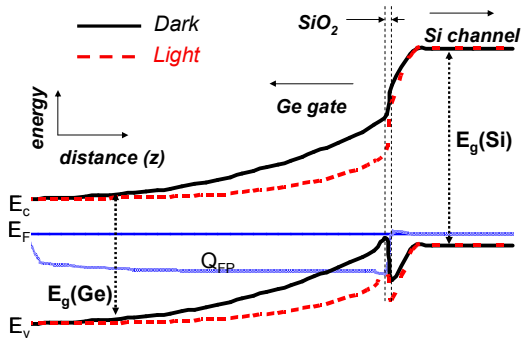
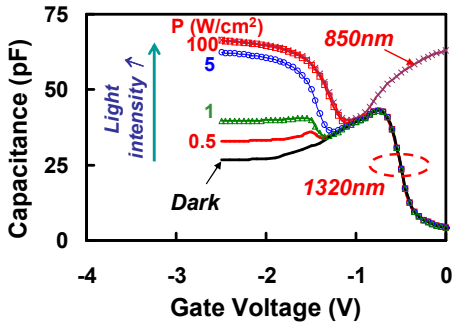
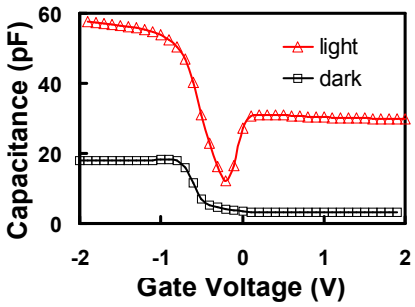


Fig. 2: Energy band diagram of Ge-SiO_2-Si stack. Equilibrium band bending is depicted by solid lines. Under illumination, bending and quasi-Fermi levels change as shown by dotted lines. Optically generated carries accumulate at either side of the gate dielectric. In the case illustrated above, holes accumulate at the Ge-SiO_2 interface, while the electrons are swept out of the gate terminal and flow to SiO_2-Si interface inducing a channel.



(a)



(b)

Fig. 3(a): Simulated C_{GATE}-V_{GATE} with varying light intensity of Ge-SiO_2-Si stack. Only Ge depletion capacitance is modulated by 1320nm light. Si also absorbs at 850nm, hence Si depletion capacitance is also modulated with this wavelength. (b): Measured high frequency (100kHz) C_{GATE}-V_{GATE} for 3.5nm thick SiO_2. Due to experimental difficulties, visible light is used in measurements. Si also absorbs at this wavelength and hence Si depletion capacitance, dominant for $V_{GATE}>0$, is also modulated.

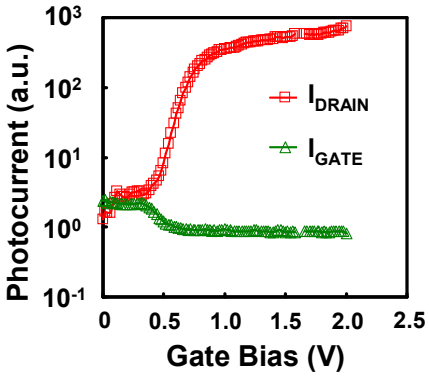


Fig. 4: Measured photocurrent at the gate and drain terminals for V_{GATE}=V_{DRAIN}. The flow of optically generated carriers in the gate constitute a gate current I_{GATE}. This current is amplified by the transistor at the drain terminal, I_{DRAIN}. Lock-in technique was used to precisely extract the optical currents.

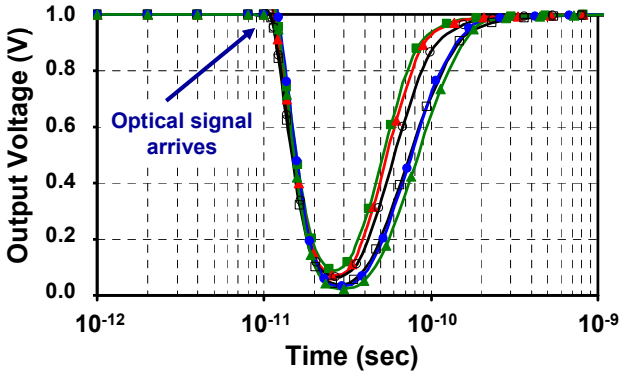


Fig. 5: Simulated transient response of two complementary optoelectronic switches driving a minimum sized electrical inverter as load. Light that acts as a gate signal arrives at 10psec. Output voltage is rail-to-rail with no amplification stages required. Family curves are plotted with changing dc gate bias.