Low-voltage broad-band electroabsorption from thin Ge/SiGe quantum wells epitaxially grown on silicon

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Abstract: We demonstrate electroabsorption contrast greater than 5 dB over the entire telecommunication S- and C-bands with only 1V drive using a new Ge/SiGe QW epitaxy design approach; further, this is demonstrated with the thinnest Ge/SiGe epitaxy to date, using a virtual substrate only 320-nm-thick. We use an eigenmode expansion method to model the optical coupling between SOI waveguides and both vertically and butt-coupled Ge/SiGe devices, and show that this reduction in thickness is expected to lead to a significant improvement in the insertion loss of waveguide-integrated devices.

OCIS codes: (230.4110) Modulators; (230.2090) Electro-optical devices; (250.3140) Integrated optoelectronic circuits; (160.2100) Electro-optical materials.

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1. Introduction

As the trend to replace metallic wire information conduits with optical links progresses to smaller distances, both inter- and intra-chip optical links are sought to alleviate the wire-interconnect bottleneck problem. Among commonly employed optoelectronic materials, Si-Ge alloys are uniquely compatible with the dominant Si CMOS technology, and Ge/SiGe quantum well systems have recently demonstrated modulation [1–5], detection [6–8], and even light-emitting [9, 10] properties.

Improving the efficiency of optical interconnects is critical to the economic and environmen-

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tal sustainability of the projected growth of data transmission needed for the rapid expansion of communication, commerce, and computation. The adoption of Si photonics technology hinges on meeting power efficiency requirements [11], and a low drive voltage (1V or less) is particularly important for CMOS compatibility and minimizing energy dissipation [12]. In addition, C-band (1530-1565 nm) wavelength modulation is desired for telecommunication, and compatibility with integrated photonic platforms requires compact form factors. High-speed devices generally require small capacitive footprints to avoid resistance-capacitance limitations, and in-plane, e.g., waveguide and microdisk active devices, should be comparable in thickness to SOI device layers.

Strong electroabsorption modulation can be obtained using multiple quantum well (MQW) layers via the quantum-confined Stark effect (QCSE) [13, 14], which is now the dominant technology for optical modulation in III-V semiconductor systems. The effect was first demonstrated in a silicon-based platform using Ge/SiGe QWs in 2005 [15] and has since been explored in a range of structural configurations including surface-normal [1], side-entry [2], waveguide [6], and microdisk [3]. However, the design and epitaxial growth of Ge/SiGe films on Si substrates are complicated by differences in lattice constants and thermal expansion coefficients.

The strain induced by the lattice mismatch between Ge and Si may be accommodated by inserting an epitaxially grown, relaxed buffer layer between the Si substrate and the QW layers. These buffer layers are necessary to facilitate the growth of mechanically stable Ge/SiGe MQW stacks by providing strain compensation, since the MQW layers would relax if epitaxially grown on a Si substrate. During crystal relaxation, misfit dislocations form, with some threading dislocations terminating at the surface. Therefore, as well as providing strain compensation, a critical function of the buffer layer is to provide a trap for misfit dislocations and reduce the threading dislocation defect density of the growth surface for the quantum well layers.

Previously demonstrated buffer layers have ranged in thickness from 500 nm to 13 μm [1, 2, 4–6, 15, 17]. However, thick buffers are not desirable due to the time and expense required to grow them and because non-planar surfaces pose difficulty for integration with CMOS. Furthermore, SOI waveguide layers employed in silicon photonic chips are typically either 220 or 400-nm-thick, and the resulting difference in thickness between the device and the access waveguide complicates the design of optical modulators. A similar problem occurs in hybrid III-V/silicon laser structures, in which the thickness difference has been circumvented by vertical coupling, rather than butt-coupling, of the active device and waveguide [18]. However, as discussed in Section 5, thin buffer layers are still preferred in the vertical coupling geometry, in order to achieve high coupling efficiencies.

In order to reduce the required epitaxy layer thickness without compromising epitaxy quality, we propose a new design for Ge/SiGe MQWs grown on Si substrates to reduce strain accumulation, preventing the formation of crystal dislocations. This is important to device performance and efficiency because such defects in the crystal structure correlate with leakage current [16]. In addition to affecting power efficiency, such conductive paths can lead to uneven electric field distribution over the QWs. This causes exciton peak broadening resulting in lower electroabsorption contrast ratios. Using this design, we show that electroabsorption contrast greater than 5 dB is possible over the entire telecommunication S- and C-bands with only 1V drive; further, this is demonstrated with the thinnest Ge/SiGe epitaxy to date, using a virtual substrate only 320-nm-thick. We have carried out simulations of the optical mode propagation in Ge/SiGe epitaxial systems on silicon, and show that this reduction in the thickness of the epitaxial layers significantly improves the optical properties of waveguide-integrated devices. Our results demonstrate the potential for room-temperature waveguide-integrated electroabsorption

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devices operating across all of the S-band and C-band with a 1V swing.

2. Thin epitaxy design

In our new structure, we have adopted an approach to improving epitaxy quality by reducing strain build-up, allowing us to develop thinner buffer layers. This is based on a more complete understanding of the strain in fabricated layers and reduction of Ge content in the SiGe film. As in previous devices, a SiGe buffer is first epitaxially grown on Si by reduced pressure chemical vapor deposition (RP-CVD). Because the lattice constant of Ge is 4% larger than that of Si, as the SiGe layer surpasses the critical thickness during growth, it becomes energetically favorable for defects to form. Defect formation relieves the strain in the film, causing it to relax with a lattice constant approaching that of unstrained SiGe. These buffer layers are homogenous and can be annealed at high temperature, unlike the heterogeneous active QW region which is grown above the buffer. In the multi-step anneal process [1,2,6,19], the buffer layers become partially relaxed during the high-temperature, sustained in-situ anneals between 750°C and 850°C.

However, during cooling, x-ray diffraction (XRD) measurement showed that the SiGe film becomes 0.18% tensile-strained, due to the larger thermal expansion coefficient of Ge and incomplete relaxation during annealing. The XRD measurement was performed on a test sample containing only epitaxial buffer layers grown according to the process described in Section 3. The XRD measurement showed that the parallel lattice constant mismatch in the SiGe buffer was found to be uniformly 38986 ppm (3.8986%) of Si, and the perpendicular lattice constant mismatch was 3.5699%. Because the ratio of in- to out-of-plane lattice constant is greater than one, the crystal is deformed by tensile strain. The percentage tensile strain (0.18%) was calculated by comparing the measured strained SiGe in-plane lattice parameter with the theoretical relaxed lattice constant (which is the same in both perpendicular and parallel directions). SiGe does not quite follow Vegard's law, so the theoretical relaxed lattice constant is calculated using $a_{SiGe\_relaxed} = a_{Si}(1+\varepsilon)$ where $\varepsilon = (a_{Si_{1-x}Ge_x} - a_{Si})/a_{Si} = 0.00501x^2 + 0.03675x$. The in-plane strain is therefore $1 - a_{SiGe\_measured}/a_{SiGe\_relaxed}$ =-0.18%, with the negative value indicating tensile strain. Additionally, a reciprocal space map (RSM) was taken of a similar test epitaxial structure, which indicated that the growth above the buffer maintained the same lattice constant as the buffer after cooling to room temperature.

This result is consistent with previous findings; the amount of tensile strain in SiGe layers grown on Si saturates at anneal temperatures above 750°C [20,21]. This can be attributed to the greater threading dislocation movement above temperatures of 780°C, which acts to relieve tensile strain as the structure cools to 780°C after a higher-temperature anneal. Without this effect, SiGe grown on Si cooled from an anneal temperature of 850°C would otherwise theoretically approach a larger tensile strain of 0.3% [20]. In the present experiments, the tensile strain found in the buffer was about 81% of the theoretical prediction of [22]. This was also consistent with prior results [20,21], and could be explained as incomplete relaxation of compressive strain in the SiGe film at the anneal temperatures used and relaxation of the tensile strain from enhanced threading dislocation movement due to thermal expansion mismatch during cooling [20,22]. Given these results, we appended an empirical prefactor of 0.81 to the expression found in [22] to more closely model the experimental results and better predict the in-plane strain, $\varepsilon_{||}$, in RP-CVD SiGe epitaxy, i.e.,

$$\varepsilon_{\|} = 0.81 \int_{T_0}^{T_1} \Big(\alpha_{SiGe}(T) - \alpha_{Si}(T)\Big) dT \tag{1}$$

where $\alpha_{SiGe}(T)$ and $\alpha_{Si}(T)$ are the temperature-dependent coefficients of thermal expansion for SiGe and Si, respectively, and $\alpha_{SiGe}(T)$ is linearly interpolated between coefficients for Si and Ge based on atomic composition.

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In contrast to previous designs for Ge QW electroabsorption devices [1, 2, 4, 6–10, 15, 17, 23, 24], which fixed the average Ge content of the QW/barrier region to that of the virtual substrate in an effort to balance strain [25], or used a strain energy minimization approach [26], our design takes into account the effect of thermal expansion on the lattice constants of epitaxial layers, and instead attempts to match the actual lattice constant of the buffer (including these empirical effects) with the average lattice constant in the rest of the structure. To do this, we use the empirical model of Eq. (1) to design our epitaxy, as shown in Table 1, using the temperature-dependent lattice constants. The outcome was that our epitaxy design has a lower atomic percentage of Ge in the regions grown above the buffer. This was consistent with the trend we have seen in previous growth experiments, in which epitaxial structures having, on average, slightly less Ge in the structure grown above the buffer outperformed structures with slightly more Ge in terms of photocurrent absorption contrast ratio.

In an effort to reduce lattice mismatch to the Si substrate and to reduce unwanted absorption in regions outside of the quantum wells, the atomic concentration of Ge in the virtual substrate was decreased from 90% to 88% compared to some previous designs. The barrier Ge content was reduced from 85% to 81%, allowing thinner barriers to be used, increasing the effective absorption coefficient of the MQW stack. At the same time, quantum confinement is increased in the Ge QWs due to the higher Si content of the barriers, helping to prevent coupling between the more closely spaced QWs.

3. Device fabrication

This epitaxial structure of Table 1 was grown on lightly p-doped <100> Si wafers using RP-CVD at a chamber pressure of 40 mTorr. The boron-doped buffer was grown in three stages. After each third of the total buffer thickness was grown at 400°C the whole structure was hydrogen annealed in-situ for 30 minutes at 800°C. The rest of the structure was grown at 400°C. Thin undoped spacers were grown before and after the QW regions to reduce dopant diffusion from the p- and n-doped regions into the active region, which consists of five nominally 12 nm Ge QWs separated by 17nm $Si_{0.19}Ge_{0.81}$ barriers.

Table 1. Epitaxy design for the Ge/SiGe QW structure grown on silicon.

Layer		**Composition**	**Doping**	**Thickness, design**	**Thickness, TEM**
n-doped cap		$Si_{0.13}Ge_{0.87}$	As 6e18cm^{-3}	60 nm	92 nm
spacer		$Si_{0.13}Ge_{0.87}$	undoped	60 nm	18 nm
QW		Ge	undoped	12 nm	14 nm
4x	barrier	$Si_{0.19}Ge_{0.81}$	undoped	17 nm	18 nm
	QW	Ge	undoped	12 nm	14 nm
spacer		$Si_{0.16}Ge_{0.84}$	undoped	40 nm	42 nm
p-doped buffer		$Si_{0.12}Ge_{0.88}$	B 4e19cm^{-3}	240 nm	320 nm
substrate		Si	p-doped	-	-

An atomic force microscope (AFM) image taken of the finished epitaxy revealed surface roughness <0.2 nm RMS (Fig. 1(a)). A cross-sectional bright-field transmission electron microscope (TEM) image of the finished structure is shown in Fig. 1(b) clearly showing the five QWs along with some crystal dislocation defects. An accurate exact threading dislocation defect count could not be obtained from the AFM or TEM, but given that they are visible within small TEM cross sections, we estimate the count to be between $3x10^7$ cm^{-2} and $1x10^{10}$ cm^{-2}.

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The apparent discrepancies between design and TEM thicknesses are noted in Table 1, and could be explained by variation in machine condition between the time of calibration and final growth run or layer thickness variation across the wafer, which can be seen even over small ranges in the TEM.

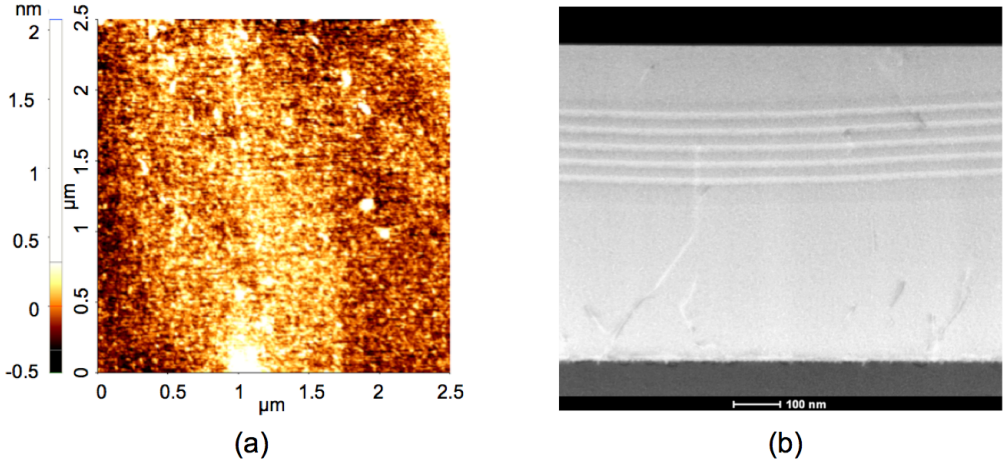

Fig. 1. (a) Surface AFM showing 0.162 nm RMS roughness. To emphasize the majority of the behavior, the color bar shows variations from -0.5 to +0.3 nm. White regions indicate positive variations beyond 0.3 nm. The minimum and maximum were -0.485 nm and 2.078 nm. (b) Cross-sectional TEM image of the epitaxial structure.

To facilitate photocurrent collection, test p-i-n diodes were fabricated by vertically dry etching square structures through the Ge/SiGe QW epitaxy down to the p-doped SiGe region to form electrically isolated devices. Ti/Pt ring contacts were deposited by electron-beam evaporation.

4. Experimental results

The devices were illuminated using a tunable laser with a lensed fiber, and photocurrent resulting from absorption was measured using a lock-in current amplifier. Photocurrent absorption spectra are shown in Fig. 2(a) for a range of DC biases. Photocurrent absorption contrast ratios with a 1-V-swing are shown in Fig. 2(b); contrast greater than 5dB (3dB) was achieved for a 1V (0.4V) swing throughout the range 1449 - 1580 nm, demonstrating for the first time that useful modulation contrast [27] is obtainable over the entire telecom S-band (1460 - 1530 nm) and C-band (1530 - 1565 nm) at room temperature using the QCSE with Ge/SiGe QWs.

The thin epitaxy improves the potential of integration with CMOS and photonic silicon-on-insulator (SOI) platforms. This reduction in the thickness of the epitaxial layers will enable significantly improved optical coupling to SOI waveguides by reducing the mismatch between the optical modes of the SOI waveguide and the Ge/SiGe epitaxial device layer. The epitaxy design was $<$560 nm, including the virtual substrate. The TEM taken from a wafer section (Table 1) estimates an as-grown thickness of 614nm. However, some of the n-doped cap could be removed by polishing using a technique similar to [5] to render the structure thickness commensurate with, or even thinner than, the design thickness.

A very important property of our present device is that good absorption contrast can be obtained with little (or no) reverse bias DC offset, or even slight forward bias. For example, we show in Fig. 2(b) a contrast of a factor of 3.45 (equivalent to 5.38 dB) in the absorption for a 1-V-swing between -0.1 V (i.e., slight forward bias) and 0.9 V reverse bias. A consequence of

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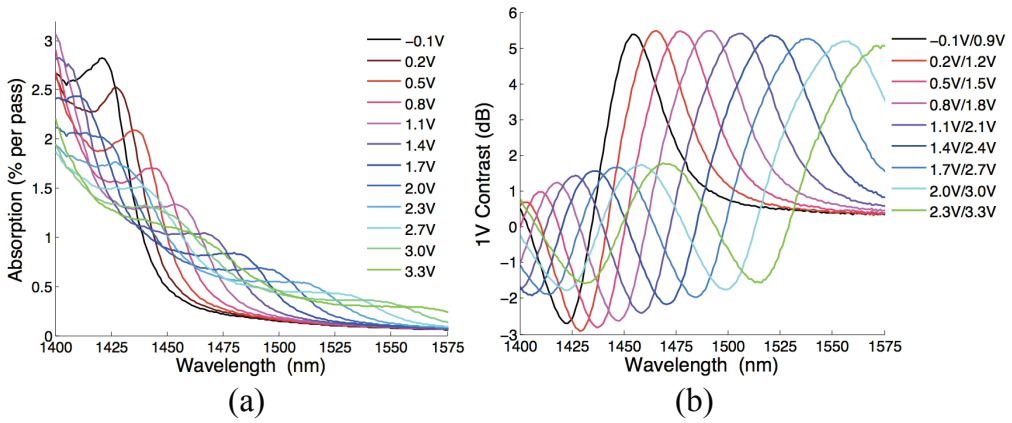

Fig. 2. (a) Absorption-per-pass spectra deduced from vertical photocurrent measurements from a 5QW Ge/SiGe QW epitaxy embedded in a diode with a 220nm intrinsic region. (b) Photocurrent absorption contrast ratios at 1V swing with biases between 0.1V forward and 2.3V reverse.

this lack of reverse bias is that the excess energy dissipation from photocurrent is substantially reduced compared to previous devices [12].

5. Discussion

5.1. Effect of epitaxy thickness on coupling losses

In order to assess the effect of the total thickness of the epitaxy on the optical coupling losses between the SOI waveguide core and the Ge/SiGe device waveguide, we performed eigenmode expansion method [28] simulations for both vertically- and butt-coupled approaches. The proposed vertically-coupled structure is illustrated in Fig. 3(a). We modeled a 600-nm-wide strip waveguide in 400-nm SOI, and used a linear taper to couple the input mode shown in Fig. 3(b) into the mode of the device section, shown in Fig. 3(c). These simulations were carried out for various device thicknesses and as a function of the length of the taper. In order to assess the coupling efficiency between the modes of the SOI waveguide core and of the device, we neglected the losses in the layers due to free carrier absorption and interband absorption. The results are shown in Fig 4. The taper length required to provide efficient mode conversion is strongly dependent on the total thickness of the epitaxial layers. Ge/SiGe MQW devices reported to date have total thicknesses of 900 nm or more [1–10, 15, 17, 23, 24], requiring a waveguide taper length of more than 100 μm to provide efficient mode coupling. However, if this total thickness can be reduced to 600 nm, we can see that the required taper length is reduced by a factor of more than two.

Alternatively, waveguide integration can be achieved using a butt-coupled geometry, whereby a recess is etched into the 400-nm-wide, 400-nm-thick Si waveguide core layer, and epitaxial growth proceeds in this recess. This scheme is similar to that described in [23], except that the recess should not be completely etched through the top Si layer: rather, a 10-nm-thick Si layer should be left on which the epitaxial growth can proceed. The resulting structure will have a discontinuity in the thickness, and the device section will be able to support multiple vertical modes, which may be excited by the fundamental mode of the incoming SOI waveguide. This leads to multi-mode interference and coherent reimaging at the output SOI waveguide, and an oscillation in the coupling loss as a function of the device length. Figure 5(a) shows the

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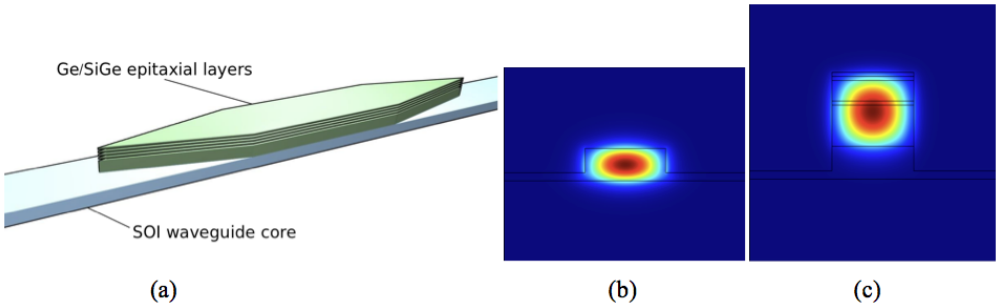

Fig. 3. (a) Schematic of the vertically-coupled lateral taper device geometry. The strip waveguide is 600-nm-wide and is etched into 400-nm-thick SOI. (b) The incoming optical mode in the SOI waveguide core is transformed into the mode in the SiGe device section (c) using the tapered mode adapters.

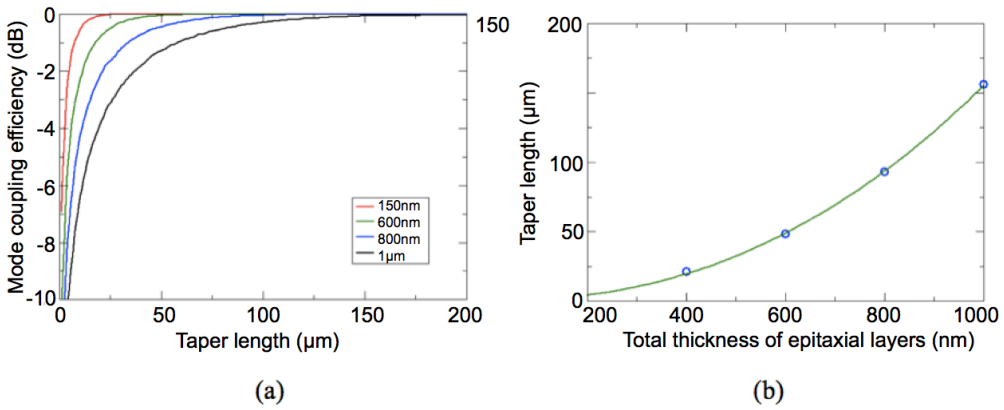

Fig. 4. (a) The coupling efficiency of the vertically-coupled lateral tapers as a function of the taper length for various total thicknesses of the Ge/SiGe epitaxial layers. (b) The taper length when the coupling loss is -0.05 dB, with a power-law fit giving an exponent of 2.28.

calculated coupling loss as a function of the device length for 900-nm-thick epitaxial layers, and Fig. 5(b) shows the coupling loss for 560-nm-thick epitaxial layers. Because the 560-nm-thick epitaxial layers support fewer vertical optical modes, the magnitude of the oscillations in the coupling loss is markedly reduced.

If we include the absorption in the different layers that arise from interband absorption in the MQW layers at the on and off bias states, as well as free-carrier absorption in the doped layers, we may determine the expected insertion loss and extinction ratio of a device based on this butt-coupled geometry. This is shown in Fig. 6(a) at 1550 nm and Fig. 6(b) at 1490 nm as a function of the length of the device, both with a 1V swing. The periodic fluctuations in the insertion loss arise from the coherent reimaging of multiple modes, and the smaller periodic fluctuation in the extinction ratio occurs because of the perturbation to the mode indices that results from the change in the absorption coefficient of MQW layers, and because the losses of the different modes may be affected differently when the loss of the MQW layer is varied. We find that, at 1550 nm, a 200-μm-long device is expected to have an extinction ratio of 6.5 dB and an insertion loss of 3.5 - 4.5 dB, depending on the exact device length. This same device is expected to have an extinction ratio of 15 dB at 1490 nm with an insertion loss of 6.5 - 8 dB.

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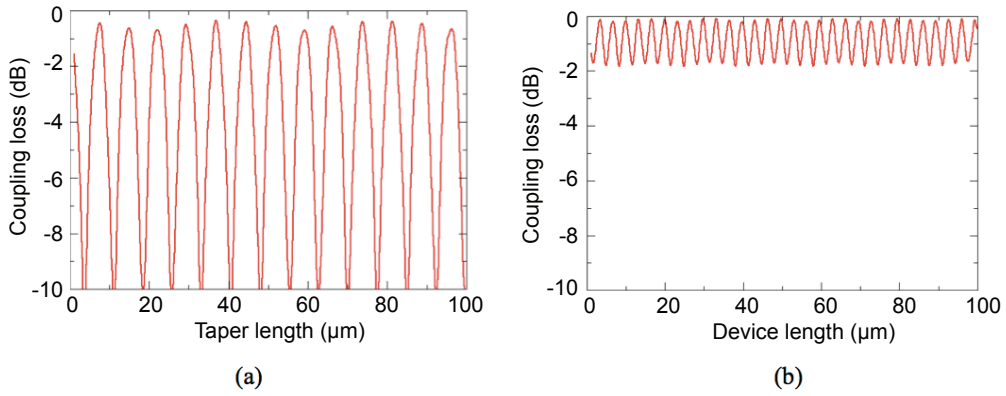

Fig. 5. (a) The optical coupling losses from a butt-coupled geometry with epitaxial layers and a total thickness of 900 nm. (b) The optical coupling losses for a butt coupled geometry with a 560-nm-thick epitaxial structure.

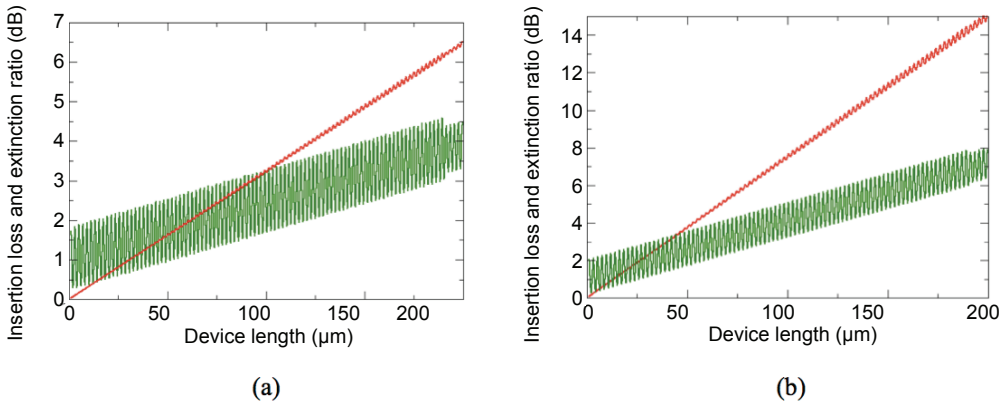

Fig. 6. The insertion loss (green) and extinction ratio (red) of the butt-coupled geometry device as a function of its length. (a) At 1550 nm and (b) at 1490 nm.

5.2. Effect of epitaxy thickness on modulator energy efficiency

The effect of photocurrent dissipation and finite contrast in modulators can be combined in one parameter [12] - an energy efficiency factor β that is the ratio of the usable optical output energy to the total electrical plus optical input energy (excluding capacitive energy) in the modulator. Using the measured absorption spectrum performance, we calculate that a β of 16% could be achieved with the present material for a mode-matched butt-coupled design that is optimized for maximum β based on the approach in [12] (here resulting in 57% transmission in the "on" state and 16% in the "off" state). Such a number is almost identical to that for the best predicted Ge QW modulator with a butt-coupled geometry so far [29]. We also expect QW modulators will have low capacitive energies. (A 0.75 fJ/bit capacitive energy has been estimated [12] for the previous Ge QW waveguide modulator demonstration [23].) Overall, such energy performance makes the Ge QW modulator comparable in energy dissipation to the best Si disk modulators (neglecting any tuning energy for those disk device) despite the absence of any resonator in the QW case. We can also expect to incorporate resonators if desired in Ge QW devices for further energy reduction, with microdisk devices [3] promising lower drive swings (e.g., 0.4V)

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and hence even lower energies.

6. Conclusion

We have demonstrated a design improvement to Ge/SiGe QWs grown by reduced pressure chemical vapor deposition with significant consequences for integrated silicon photonic modulators. We show in one thin QCSE modulator diode structure that useful modulation is possible throughout the entire telecommunication S- and C-bands, and with less than 1V total drive voltage. This low drive voltage is particularly important for minimizing energy dissipation [12]. Because of optimized buffer layers, unlike previous Ge QW diode structures, the epitaxy is also thin enough that it may enable a variety of new device structures, including thin waveguides, disks and photonic crystals. Simulations predicted that the demonstrated reduction in epitaxy thickness will significantly improve the efficiency of waveguide-integrated modulator devices. Vertically-coupled geometries will benefit from decreased taper lengths and hence smaller capacitive footprints leading to greater energy effiency, and both vertically- and butt-coupled waveguide modulators will benefit from reduced coupling losses.

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